INTRODUCTION TO CPU

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Session 2 Microprocessor Course
Isfahan University of Technology
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Agenda

• Review of the first session
• A tour of silicon world!
• Basic definition of CPU
• Von Neumann Architecture
  • Example: Basic ARM7 Architecture
  • A brief detailed explanation of ARM7 Architecture
• Harvard Architecture
  • Example: TMS320C25 DSP
Agenda (2)

- History of CPUs
  - 4004
  - TMS1000
  - 8080
  - Z80
  - Am2901
  - 8051
  - PIC16
Von Neumann Architecture

- Same Memory
  - Program
  - Data
- Single Bus
Sample: ARM7T CPU
Harvard Architecture

- Separate memories for program and data
TMS320C25 DSP

[Diagram of TMS320C25 DSP with labels and connections]
## Silicon Market

<table>
<thead>
<tr>
<th>Rank 2009</th>
<th>Rank 2008</th>
<th>Company</th>
<th>Country of origin</th>
<th>Revenue (million $ USD)</th>
<th>2009/2008 changes</th>
<th>Market share</th>
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<tr>
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<td>Hynix</td>
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<td>Sony</td>
<td>Japan</td>
<td>4 468</td>
<td>-35.7%</td>
<td>1.9%</td>
</tr>
</tbody>
</table>
Silicon Market (2)

• Total 2009 sales
  • 229,917,000,000 US$
• 2009 sales growth: -11.7%
• Total 2008 sales
  • 258,304,000,000 US$
Intel 4004 (1)
Intel 4004 (2)

- 1971
- Just a calculator (not for industry)
- 4-bits CPU
  - ALU: 4bits
  - Instructions: 8bits
- Separate program and Data memories
  - 1K data memory
  - 4K program memory
    - PC width?
Intel 4004 (3)

- Registers
  - Sixteen 4 bits registers
- Stack
  - 4 Level stack
- Instructions
  - 46
- Clock frequency : 740kHz
- 2300 transistors
- Speed : 92,000 instructions per second
Intel 4004 (4)
Intel 4004 (5)

- Single multiplexed 4 bit bus:
  - 12 bit addresses
  - 8 bit instructions
  - 4 bit data
Intel 4004 (6)

• Supported Chips:
  • 4001: 256Bytes ROM
  • 4002: 40Bytes RAM
  • 4003: 10bit shift register
  • 4008: 8bit address latch
  • 4009: programmed I/O access
  • 4269: keyboard, display interface
Texas Instruments TMS1000
Texas Instruments TMS1000 (2)
Texas Instruments TMS1000 (3)

- 1974
- First Micro-controller
  - Computer on a chip
  - MPU, RAM, ROM, Timers
- Clock
  - 300KHz
- Address space
  - 1KB
Texas Instruments TMS1000 (4)

- RAM
  - 32 Bytes
- ROM
  - 1KBytes
- Instructions
  - 31
- Registers: different size each!
- PC: not a counters, but a shift register!
Intel 8080

- 1974
- 8bits CPU
- Buses
  - 16bits address bus
    - What range?
  - 16bits PC
  - 16bits Stack Pointer
  - 8bits data bus
- 7 registers : 8bits each
Intel 8080 (2)

- Some registers could join to make 16bits registers
- Separate
  - Memory port
    - To talk to external memory
  - I/O port
    - To talk to external peripherals and devices
- Update: 8085 (1976)
  - Added interrupt pins and serial I/O pins
Zilog Z80

- 1976
- An improved 8080
  - 80 additional instructions
    - Block move instructions
    - Bit manipulation
  - 2 Register banks
    - Suitable for interrupt handling
- Federico Faggin
  - Left Intel at 1974
  - After his work on 8080
  - Founded Zilog
Zilog Z80 (2)

- **Clock Frequency:**
  - 2.5MHz to 20 MHz (NMOS to CMOS)

- **Memory interface**
  - Z80 capable of generating DRAM refresh signals itself

- **CP/M**
  - First operating system for microprocessors
  - Mainly designed for 8080
  - Z80 and 8080 were code compatible

- **Extensions to Z-80**
  - Z180, Z280, Z800
  - eZ80 : 24bits core
Zilog Z80 (3)
Zilog Z80 (4)
Zilog Z80 (5)

• Registers
  • A : Accumulator
  • F : Flags
    • Carry, Zero, Parity, ...
  • BC, DE, HL : 8/16bits registers
    • 8bits for computations
    • 16bits for address generation
  • SP : 16bits stack pointer
  • PC : 16bits program counter
  • IX , IY : 16bit index register
  • R : 8bits DRAM refresh counter
    • I : 8bits interrupt vector, base register
• Shadow registers : AF’, BC’, DE’, HL’
Zilog Z80 (6)

- Addressing modes:
  - Immediate:
    - LD A,FFH
    - LD HL,1234H
  - Page zero (used for jumps and calls)
  - Relative (used for jumps and calls)
  - Extended addressing (used for jumps and calls)
  - Indexed addressing
    - LD A,(IX+1)
    - LD A,(IY-4)
  - Register indirect addressing
    - LD A,(HL)
Zilog Z80 (7)

The assembly program:

```
ORG 100H ;Locate program at 100H
LD HL,1234H ;Address of first number
LD A,(HL) ;Operand 1 into Accu
INC HL ;Address of 2nd number
ADD A,(HL) ;Addition
INC HL ;Address of result (sum)
LD (HL), A ;store result
END ;end of program

ORG 1234H ;Location of the data
DB 100,200 ;put 64H and C8H
```
Zilog Z80 (8)

- Instruction: LD A,(HL)
Zilog Z80 (9)

- Instruction: OUT n,A
AMD AM2901

- 4bits CPU
  - 4-bit-slice processor
- Contained ALU and control signals
  - 8bit ALU consists of two 4bits ALU
- 16 registers 4bits each
- AM2903 : contained multiply operation
- AMD9511 : First floating point coprocessor
  - 1979
  - 32bits operations
Intel MCS-51

- 1977
- Microcontroller
  - On-chip RAM and ROM
- 2bytes instruction set
- Over 1Billion sold from 1988
- Extensions by Siemens and TI
- Available widely today
  - In different forms
Intel MCS-51 (2)

- Four separate register sets
- Internal static RAM:
  - 80C51 : 128 Bytes
  - 80C52 : 256 Bytes
  - Address Range : 0x0 – 0xff
    - 0x0 – 0x7f : can be accessed directly (128bytes)
      - Example: MOV A, 30h
    - 0x7f – 0xff : should be accessed indirectly
      - Example: MOV A, @R0
    - 0x7f – 0xff : Are control registers of 8051 (Special Function Registers)
  - 0x20 – 0x2f : bit accessible
- Internal program memory
- Support for external memory
MCS-51 Internal Memory

<table>
<thead>
<tr>
<th>IRAM Addr</th>
<th>R0</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
<th>R4</th>
<th>R5</th>
<th>R6</th>
<th>R7</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
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<tr>
<td>08</td>
<td>R0</td>
<td>R1</td>
<td>R2</td>
<td>R3</td>
<td>R4</td>
<td>R5</td>
<td>R6</td>
<td>R7</td>
</tr>
<tr>
<td>10</td>
<td>R0</td>
<td>R1</td>
<td>R2</td>
<td>R3</td>
<td>R4</td>
<td>R5</td>
<td>R6</td>
<td>R7</td>
</tr>
<tr>
<td>18</td>
<td>R0</td>
<td>R1</td>
<td>R2</td>
<td>R3</td>
<td>R4</td>
<td>R5</td>
<td>R6</td>
<td>R7</td>
</tr>
<tr>
<td>20</td>
<td>00</td>
<td>08</td>
<td>10</td>
<td>18</td>
<td>20</td>
<td>28</td>
<td>30</td>
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<td>28</td>
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<td></td>
</tr>
</tbody>
</table>

**Description**

- Reg. Bank 0
- Reg. Bank 1
- Reg. Bank 2
- Reg. Bank 3
- Bits 00-3F
- Bits 40-7F
- General User RAM & Stack Space (80 bytes, 30h-7Fh)
- General IRAM
- Special Function Registers (SFRs) (80h - FFh)
- SFRs
MCS-51 Internal Memory
MCS-51 Bit Memory

• Addresses : 20H – 30H
• Bit Address: 00H – 7FH (128bits total)
• Instruction sample:
  • SETB 24H
  • CLR 25H
  • MOV 20H,#0FFH
    • Equivalent to 8 SETB operations
• Bit Address: 80H – FFH
  • Used for accessing SFR
  • Example:
    • MOV P0,#01
    • SETB 80H
MCS-51 (3)

- Supported Peripherals
  - UART
    - universal asynchronous receiver transmitter
    - Serial interface (TX/RX)
  - Timers
    - time measurement
    - Make an event happen in a specified intervals
  - I2C
    - inter-integrated circuit bus
    - Multi-master bus
    - Mainly to transfer control data
  - SPI
    - Serial peripheral interconnect
    - Serial data transfer for memories
MCS-51 (4)

- Supported peripherals (2)
  - USB
    - Peripheral
    - Host
- CAN
  - Controller-area network
  - A bus to allow microcontrollers talk to each other in a vehicle
  - Without a host computer
  - Now also used in industrial automation and medical equipment
- PWM generator
  - Generate PWM pulses
MCS-51 (5)

- Supported Peripherals
  - Analog comparator
  - A/D and D/A
  - RTC
    - A computer clock
    - Keeps track of the current time
    - Keeps accurate time and date
### MCS-51 Special Function Registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
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<tr>
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<td>P0</td>
</tr>
<tr>
<td>81</td>
<td>SP</td>
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<tr>
<td>82</td>
<td>DPL</td>
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<td>83</td>
<td>DPH</td>
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<td>84</td>
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<td>88</td>
<td>TL1</td>
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<td>SCON</td>
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<td>IE</td>
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<td>94</td>
<td>P2</td>
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<td>95</td>
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<td>96</td>
<td>P3</td>
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<td>97</td>
<td>B</td>
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<tr>
<td>A0</td>
<td>C</td>
</tr>
<tr>
<td>A1</td>
<td>D</td>
</tr>
<tr>
<td>A2</td>
<td>E</td>
</tr>
<tr>
<td>A3</td>
<td>F</td>
</tr>
<tr>
<td>A4</td>
<td>PSW</td>
</tr>
<tr>
<td>A5</td>
<td>ACC</td>
</tr>
<tr>
<td>A6</td>
<td>B</td>
</tr>
</tbody>
</table>

- **Blue background** are I/O port SFRs
- **Yellow background** are control SFRs
- **Green background** are other SFRs
MCS-51 Ports

- 8051/52 has 4 ports
  - General purpose I/O
  - P0, P1, P2, P3

- Using external memory:
  - Program is stored outside 8051
  - P0 & P2 will be used for memory interfacing
MCS-51 Stack Pointer

- SP points to the tail of the stack
- PUSH A
  - SP ← SP+1
  - Value A will be stored in memory address : SP
- POP A
  - Value A will be read from memory address : SP
  - SP ← SP – 1
- Instructions that change SP:
  - CALL, RET, POP, PUSH, interrupts
MCS-51 SFRs

- **DPL/DPH** : DPTR , Data pointer
  - 16bits register
  - Used for addressing external operands
- **PCON** : Power control
  - Sleep mode
- **TCON** : Timer control
  - Stop, start , overflow...
- **TMOD** : Timer mode
  - 16bits timers/13bits/ two separate 8bits
  - Count what? Events? External pin changes?
- **TL0/TH0 , TL1/TH1** : Timers
  - Always count up
MCS-51 SFRs (2)

- SCON: serial control
  - Baud rate
  - Start/stop
  - Flags
- SBUF: serial port data buffer
- IE: Interrupt enable
- IP: interrupt priority
  - Example: High priority for serial interrupt
- PSW: program status word
  - Carry flag, overflow flag, parity flag,…
  - Register bank select bits
- ACC: Accumulator
  - MOV E0H,#20h == MOV A,#20h
- B: used for divide and multiply operations
MCS-51 Addressing Modes

- Immediate addressing
  - MOV A,#20h
- Direct Addressing
  - MOV A,30h
- Indirect Addressing
  - MOV A,@R0
- External Addressing
  - MOVX A,@DPTR
- Code Indirect
  - MOVC A,@DPTR
Intel MCS-51
Microchip Corporation

• Created 1987
  • A “General Instrument” company spin off

• Products
  • Micro-controllers
    • PIC16/18
    • PIC24/32
    • dsPIC
  • Serial storage :
    • Serial EEPROM
    • Serial SRAM
  • USB controllers
  • ZigBee interfaces
Microchip PIC

- 1975
- PIC : Programmable Interface Controller
- Designed in Harvard University
  - To be used in a commercial product
  - In “General Instrument” company
- A new company born
  - Arizona Microchip Technology
- 2008:
  - Microchip announced its six billionth PIC processor shipment
PIC Micro-controllers

- No difference between
  - Memory space
  - Register space
  - RAM serves as: memory & registers

- Banking mechanism
  - Extend addressing range
  - Data transfers should happen within a bank
    - Or accumulator should be used as temporary storage
  - Later versions
    - Move instructions
    - Capable of addressing whole memory range

- Generally
  - No external memory interface
  - Exception: PIC17 & high pin count PIC18
  - Shadow registers in PIC18 for interrupts
Code Space

- ROM
- EPROM
- Flash ROM

Addressing in program memory:
- Is not based on Bytes
- Depends on length of instructions
- For example:
  - Each memory cell is 12Bits
  - There are total number of 128cells of 12Bits each
  - Example: 4096*14bits for 16F690

- Stack
  - Is not accessible from software

- PIC18
  - Byte addressable memory
  - Software based stack
PIC Performance

- Each instruction
  - Takes 2 instruction cycle to execute
- Execution time
  - Number of instructions * 2
- Interrupt latency is constant
  - 3 instruction cycles
- Measuring performance of a portion of code:
  - Profiling
Real-time system

• A system
  • Which should produce response to input
  • In a specified amount of time

• Profiling
  • Important in making real-time systems

• A program that performs profiling:
  • Profiler

• Every CPU architecture
  • Has its own profiler

• Example:
  • Intel VTune Performance Analyzer
PIC Compilers

- C compiler
- 2008
  - Microchip announced their own compiler
  - For 18F, 24F and 30F devices
- In contrast
  - Atmel AVR
    - Supported by GNU C compiler
PIC10 & PIC16

• PIC16x
  • 33 fixed length 12bits instructions (RISC)
  • 32Bytes register file
  • 2 level deep call stack
  • First 7 to 9 bytes of register file: special purpose registers
  • Bank number : higher 3bits of FSR
  • Registers 0-15 are global
    • Not affected by bank select bits
  • Registers 16-31
    • Will change by bank select bits
Microchip PIC17/18

• PIC17x
  • 16Bits op-codes
  • 16 level deep call stack
  • Read access to code memory
  • Direct register to register moves
  • External program memory interface
  • Single-cycle 8bits multiply
  • 64K-word program space (2K to 8K on chip)

• PIC18x
  • We will have a close look later
dsPIC and PIC24

- 16bits micro-controllers
- Mass production: 2004
- dsPIC: digital signal processing capabilities

Features
- Added 16 registers
- Stack in RAM
- Direct access to data in program memory
- Interrupt sources may be assigned to handlers
  - Interrupt vector table
dsPIC

- Supported by: GNU C compiler
- Support for
  - Hardware MAC
    - Single cycle 16X16 multiplication
  - Barrel shifter
  - Direct Memory Access operations

- We will talk about capabilities of DSP chips in depth later!
PIC32

- 2007
- Based on MIPS32 M4K Core
- Supported by GCC
- …
Intel 80x86

- 1978
- 16Bits CPU
- 1979 : Intel 8088
  - The same architecture as 8086
  - 8Bits data bus instead of 16Bits bus
  - Used in first IBM PC
- Clock frequency: 5 – 10MHz
At the time of 8086

- Intel 8085 (1977)
- Motorola 6800 (1974)
- Microchip PIC16X (1975)
- MOS Technology 6502 (1975)
- Zilog Z80 (1976)
- Motorola 6809 (1978)
8086

- Project: Spring 1976 – Summer 1978
- Backward compatible
  - 8008, 8080, 8085
- Support for
  - Full 16Bits processing
- Base + Offset addressing
- Self repeating operations
- Micro-coded Multiply & Divide
- Bus structure adapted to co-processors
  - 8087 / 8089
Area & Naming

- 20,000 transistors
- Naming
  - Used in most of the later CPUs
  - 80286, 80386, 80486, 80586 …
8086 pin out
8086 Modes

• 8086 Minimum Mode
  • Normal mode of operation
  • One CPU is connected to other peripherals

• 8086 Maximum Mode
  • Used when there are multiple processors in system
  • Bus control signals by 8288 bus controller

• IBM/PC
  • Maximum mode
  • CPU + co-processor
# 8086 Registers

## Main registers

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
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<tbody>
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<td>AH</td>
<td>AL</td>
<td>AX</td>
</tr>
<tr>
<td>BH</td>
<td>BL</td>
<td>BX</td>
</tr>
<tr>
<td>CH</td>
<td>CL</td>
<td>CX</td>
</tr>
<tr>
<td>DH</td>
<td>DL</td>
<td>DX</td>
</tr>
</tbody>
</table>

**AX** (primary accumulator)

**BX** (base, accumulator)

**CX** (counter, accumulator)

**DX** (accumulator, other functions)

## Index registers

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SI</td>
<td>Source Index</td>
</tr>
<tr>
<td>DI</td>
<td>Destination Index</td>
</tr>
<tr>
<td>BP</td>
<td>Base Pointer</td>
</tr>
<tr>
<td>SP</td>
<td>Stack Pointer</td>
</tr>
</tbody>
</table>

**Source Index**

**Destination Index**

**Base Pointer**

**Stack Pointer**
# 8086 Registers

<table>
<thead>
<tr>
<th>Status register</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1 5 1 4 1 3 1 2 1 1 1 0 9 8 7 6 5 4 3 2 1 0</td>
<td>(bit position)</td>
</tr>
<tr>
<td>- - - - - O D I T S Z - A - P - C</td>
<td>Flags</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Segment register</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CS</td>
<td>Code Segment</td>
</tr>
<tr>
<td>DS</td>
<td>Data Segment</td>
</tr>
<tr>
<td>ES</td>
<td>Extra Segment</td>
</tr>
<tr>
<td>SS</td>
<td>Stack Segment</td>
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</table>

<table>
<thead>
<tr>
<th>Instruction pointer</th>
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</tr>
</thead>
<tbody>
<tr>
<td>IP</td>
<td>Instruction Pointer</td>
</tr>
</tbody>
</table>
8086 Flags

- **O**: Overflow
  - Set when MSB is set or cleared
- **D**: Direction
  - Direction of string operation
- **I**: interrupt enable
  - Set this, enable maskable interrupts
  - NMI is always active
- **T**: single step flag
- **S**: sign
  - Set when MSB of the result is set
- **Z**: Zero flag
- **A**: Some kind of carry
- **P**: Parity flag
  - Set if number of 1 is even
- **C**: Carry flag
  - Set if carry from MSB, or Borrow to MSB happened
Segmentation

• Registers : 16Bits
• External address bus: 20Bits
• Address generation:
  • Segment Register $\ll 4 + \text{Offset Register}$
• Could address 1MBytes
• Pointers
  • Near : inside a segment
  • Far : every where!
Memory Models

- Compilers
  - Different memory models for programs
  - To specify default pointer size
- Tiny (max 64kbytes)
- Small (128kbytes)
- Compact (data > 64kbytes)
- Medium (code > 64kbytes)
- Large (code, data > 64kbytes)
- Huge (arrays > 64kbytes)
8086

- Separate Memory and I/O space
  - 64kbyte I/O space
- Multiplexed address and data bus
  - Limited performance
- 256 Interrupts
Co-Processors

- 8086
  - Capable of connecting to co-processor chips
  - Floating point calculations
- 8087
  - Math co-processor
  - 80bit values
Compatible Versions

- By
  - Fujitsu
  - Harris/Intersil
  - OKI
  - Siemens
  - Texas Instruments
  - NEC
  - Mitsubishi
  - AMD
  - Soviet Union
Intel 8087

- 1980
- First floating point co-processor for 8086
- 45,000 transistors
- Computation performance
  - 50,000 FLOPS
- 8087 can be paired with 8086, 8088
- All 8087 Assembly instructions begin with
  - FADD, FMUL, FCOM
- All 8087 op-codes begin with
  - 11011 pattern (27 decimal)
Intel 8087

- Registers
  - Not addressable directly

- 8 registers
  - Make a stack
  - 8 levels deep
  - Each register: 80 bits
  - St0 to st7

- Design of 8087
  - Basis of IEEE 754 standard
  - 80387: first co-processor meeting IEEE standard completely

- Data types in 8087
  - 32/64/80 Bits
8087 Instruction Execution

- 8087
  - Directly connected to Data and Address buses of 8086 CPU
- 8086
  - Gives control to 8087
  - When it encounters instructions that begin with 27
  - 8087 gives the control back when finished with operations
- Later co-processors
  - Did not connect to buses directly
  - Instruction was given by CPU itself
A BRIEF LOOK…

CHAPTER 2
Logic Gates

• NOT
  • 2 transistors
• FET switches
  • Built using Silicon
  • Not ideal
• Leakage current
• Manufacturing technology
• Clock frequency
## Transistor Count

<table>
<thead>
<tr>
<th>Function</th>
<th>Transistor count</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT</td>
<td>2</td>
</tr>
<tr>
<td>BUF</td>
<td>4</td>
</tr>
<tr>
<td>NAND 2-input</td>
<td>4</td>
</tr>
<tr>
<td>XOR 2-input</td>
<td>6</td>
</tr>
<tr>
<td>XNOR 2-input</td>
<td>8</td>
</tr>
<tr>
<td>NOT MUX 2-input</td>
<td>8</td>
</tr>
<tr>
<td>MUX 4-input</td>
<td>24</td>
</tr>
<tr>
<td>Adder full</td>
<td>28</td>
</tr>
<tr>
<td>Latch, D gated</td>
<td>8</td>
</tr>
<tr>
<td>Flip-flop, edge triggered dynamic D with reset</td>
<td>12</td>
</tr>
</tbody>
</table>
## CPU transistor count (1)

<table>
<thead>
<tr>
<th>Processor</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel 4004</td>
<td>2,300</td>
<td>1971</td>
<td>Intel</td>
<td>10 µm</td>
<td></td>
</tr>
<tr>
<td>Intel 8008</td>
<td>3,500</td>
<td>1972</td>
<td>Intel</td>
<td>10 µm</td>
<td></td>
</tr>
<tr>
<td>MOS Technology</td>
<td>3,510</td>
<td>1975</td>
<td>MOS Technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6502</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intel 8080</td>
<td>4,500</td>
<td>1974</td>
<td>Intel</td>
<td>6 µm</td>
<td></td>
</tr>
<tr>
<td>Intel 8088</td>
<td>29,000</td>
<td>1979</td>
<td>Intel</td>
<td>3 µm</td>
<td></td>
</tr>
<tr>
<td>Intel 80286</td>
<td>134,000</td>
<td>1982</td>
<td>Intel</td>
<td>1.5 µm</td>
<td></td>
</tr>
</tbody>
</table>
## CPU transistor count (2)

<table>
<thead>
<tr>
<th>Microprocessor</th>
<th>Transistor Count</th>
<th>Year</th>
<th>Manufacturer</th>
<th>Technology Node</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel 80386</td>
<td>275,000</td>
<td>1985</td>
<td>Intel</td>
<td>1.5 µm</td>
</tr>
<tr>
<td>Intel 80486</td>
<td>1,180,000</td>
<td>1989</td>
<td>Intel</td>
<td>1 µm</td>
</tr>
<tr>
<td>Pentium</td>
<td>3,100,000</td>
<td>1993</td>
<td>Intel</td>
<td>0.8 µm</td>
</tr>
<tr>
<td>AMD K5</td>
<td>4,300,000</td>
<td>1996</td>
<td>AMD</td>
<td>0.5 µm</td>
</tr>
<tr>
<td>Pentium II</td>
<td>7,500,000</td>
<td>1997</td>
<td>Intel</td>
<td>0.35 µm</td>
</tr>
</tbody>
</table>
## CPU transistor count (3)

<table>
<thead>
<tr>
<th>Model</th>
<th>Transistor Count</th>
<th>Year</th>
<th>Manufacturer</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMD K6</td>
<td>8,800,000</td>
<td>1997</td>
<td>AMD</td>
<td>0.35 µm</td>
</tr>
<tr>
<td>Pentium III</td>
<td>9,500,000</td>
<td>1999</td>
<td>Intel</td>
<td>0.25 µm</td>
</tr>
<tr>
<td>AMD K6-III</td>
<td>21,300,000</td>
<td>1999</td>
<td>AMD</td>
<td>0.25 µm</td>
</tr>
<tr>
<td>AMD K7</td>
<td>22,000,000</td>
<td>1999</td>
<td>AMD</td>
<td>0.25 µm</td>
</tr>
<tr>
<td>Pentium 4</td>
<td>42,000,000</td>
<td>2000</td>
<td>Intel</td>
<td>180 nm</td>
</tr>
<tr>
<td>Atom</td>
<td>47,000,000</td>
<td>2008</td>
<td>Intel</td>
<td>45 nm</td>
</tr>
<tr>
<td>Barton</td>
<td>54,300,000</td>
<td>2003</td>
<td>AMD</td>
<td>130 nm</td>
</tr>
<tr>
<td>AMD K8</td>
<td>105,900,000</td>
<td>2003</td>
<td>AMD</td>
<td>130 nm</td>
</tr>
<tr>
<td>Itanium 2</td>
<td>220,000,000</td>
<td>2003</td>
<td>Intel</td>
<td>130 nm</td>
</tr>
<tr>
<td>Cell</td>
<td>241,000,000</td>
<td>2006</td>
<td>Sony/IBM/Toshiba</td>
<td>90 nm</td>
</tr>
</tbody>
</table>
### CPU transistor count (4)

<table>
<thead>
<tr>
<th>Model</th>
<th>Transistor Count</th>
<th>Year</th>
<th>Company</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core 2 Duo</td>
<td>291,000,000</td>
<td>2006</td>
<td>Intel</td>
<td>65 nm</td>
</tr>
<tr>
<td>AMD K10</td>
<td>463,000,000</td>
<td>2007</td>
<td>AMD</td>
<td>65 nm</td>
</tr>
<tr>
<td>AMD K10</td>
<td>758,000,000</td>
<td>2008</td>
<td>AMD</td>
<td>45 nm</td>
</tr>
<tr>
<td>Itanium 2, with 9MB cache</td>
<td>592,000,000</td>
<td>2004</td>
<td>Intel</td>
<td>130 nm</td>
</tr>
<tr>
<td>Core i7 (Quad)</td>
<td>731,000,000</td>
<td>2008</td>
<td>Intel</td>
<td>45 nm</td>
</tr>
<tr>
<td>POWER6</td>
<td>789,000,000</td>
<td>2007</td>
<td>IBM</td>
<td>65 nm</td>
</tr>
<tr>
<td>Six-Core Opteron 2400</td>
<td>904,000,000</td>
<td>2009</td>
<td>AMD</td>
<td>45 nm</td>
</tr>
</tbody>
</table>
## CPU transistor count (5)

<table>
<thead>
<tr>
<th>Model</th>
<th>Transistor Count</th>
<th>Year</th>
<th>Manufacturer</th>
<th>Process Technology</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>Six-Core Six-Core Core i7</td>
<td>1,170,000,000</td>
<td>2010</td>
<td>Intel</td>
<td>32 nm</td>
<td></td>
</tr>
<tr>
<td>Dual-Core Dual-Core Itanium 2</td>
<td>1,700,000,000³</td>
<td>2006</td>
<td>Intel</td>
<td>90 nm</td>
<td>596 mm²</td>
</tr>
<tr>
<td>Six-Core Six-Core Xeon 7400</td>
<td>1,900,000,000</td>
<td>2008</td>
<td>Intel</td>
<td>45 nm</td>
<td></td>
</tr>
<tr>
<td>Quad-Core Quad-Core Itanium Tukwila</td>
<td>2,000,000,000⁴</td>
<td>2010</td>
<td>Intel</td>
<td>65 nm</td>
<td></td>
</tr>
<tr>
<td>8-Core 8-Core Xeon Nehalem-EX</td>
<td>2,300,000,000⁵</td>
<td>2010</td>
<td>Intel</td>
<td>45 nm</td>
<td></td>
</tr>
</tbody>
</table>
## GPU transistor count

<table>
<thead>
<tr>
<th>Processor</th>
<th>Transistor count</th>
<th>Date of introduction</th>
<th>Manufacturer</th>
<th>Process</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>G80</td>
<td>681,000,000</td>
<td>2006</td>
<td>NVIDIA</td>
<td>90 nm</td>
<td>480 mm²</td>
</tr>
<tr>
<td>RV770</td>
<td>956,000,000</td>
<td>2008</td>
<td>AMD</td>
<td>55 nm</td>
<td>260 mm²</td>
</tr>
<tr>
<td>RV850</td>
<td>1,040,000,000</td>
<td>2009</td>
<td>AMD</td>
<td>40 nm</td>
<td>170 mm²</td>
</tr>
<tr>
<td>GT200</td>
<td>1,400,000,000</td>
<td>2008</td>
<td>NVIDIA</td>
<td>55 nm</td>
<td>576 mm²</td>
</tr>
<tr>
<td>RV870</td>
<td>2,154,000,000</td>
<td>2009</td>
<td>AMD</td>
<td>40 nm</td>
<td>334 mm²</td>
</tr>
<tr>
<td>GF100</td>
<td>3,000,000,000</td>
<td>2010</td>
<td>NVIDIA</td>
<td>40 nm</td>
<td>529 mm²</td>
</tr>
</tbody>
</table>
Gordon Moore

- The co-founder of Intel
- Famous
  - Because of Moore’s law
Moore’s Law (1)

- 1965
- Number of transistors
  - In commercial CPUs
  - Will be almost DOUBLED
  - Every two years
- In other words
  - Number of transistors per chip:
  - $2^{\text{year} - 1959}$
Moore’s Law (2)

• Number of designers for each CPU
  • Grows as 1/x
  • 4004 had 3 designers
  • Intel dual core has 300 designers

• Fab cost
  • Grows as 1/x
  • 90nm fab costs 2 Billion dollars
Moore’s Law in Practice

CPU Transistor Counts 1971-2008 & Moore’s Law

Curve shows ‘Moore’s Law’: transistor count doubling every two years
Improving Performance

• How to improve performance
  • Increase transistor count
    • Cache area
    • Parallel units
  • Increase frequency
NOT Gate Power Consumption

\[ V_{cc} \]

\[ V_{out} \]

\[ V_{in} \]

\[ V_{cc} \]

\[ I_{max} \]

\[ I_D \]
CPU Power Consumption

Power Density

- Rocket Nozzle
- Nuclear Reactor
- Hot Plate
- IBM 4004
- IBM 8080
- IBM 8085
- IBM 386
- IBM 486
- IBM P6
- Pentium®
- Sun’s Surface

...chips might become hot...
Generated Heat

- Generated Heat is a function of:
  - $F$: Running frequency
  - $V^2$: Supply voltage to the power of 2
- We have to decrease these variables
Intel CPU Trends
(sources: Intel, Wikipedia, K. Olukotun)
MULTI CORE COMPUTING

Chapter 3