INTRODUCTION TO CPU

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Session 2 Microprocessor Course

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Agenda

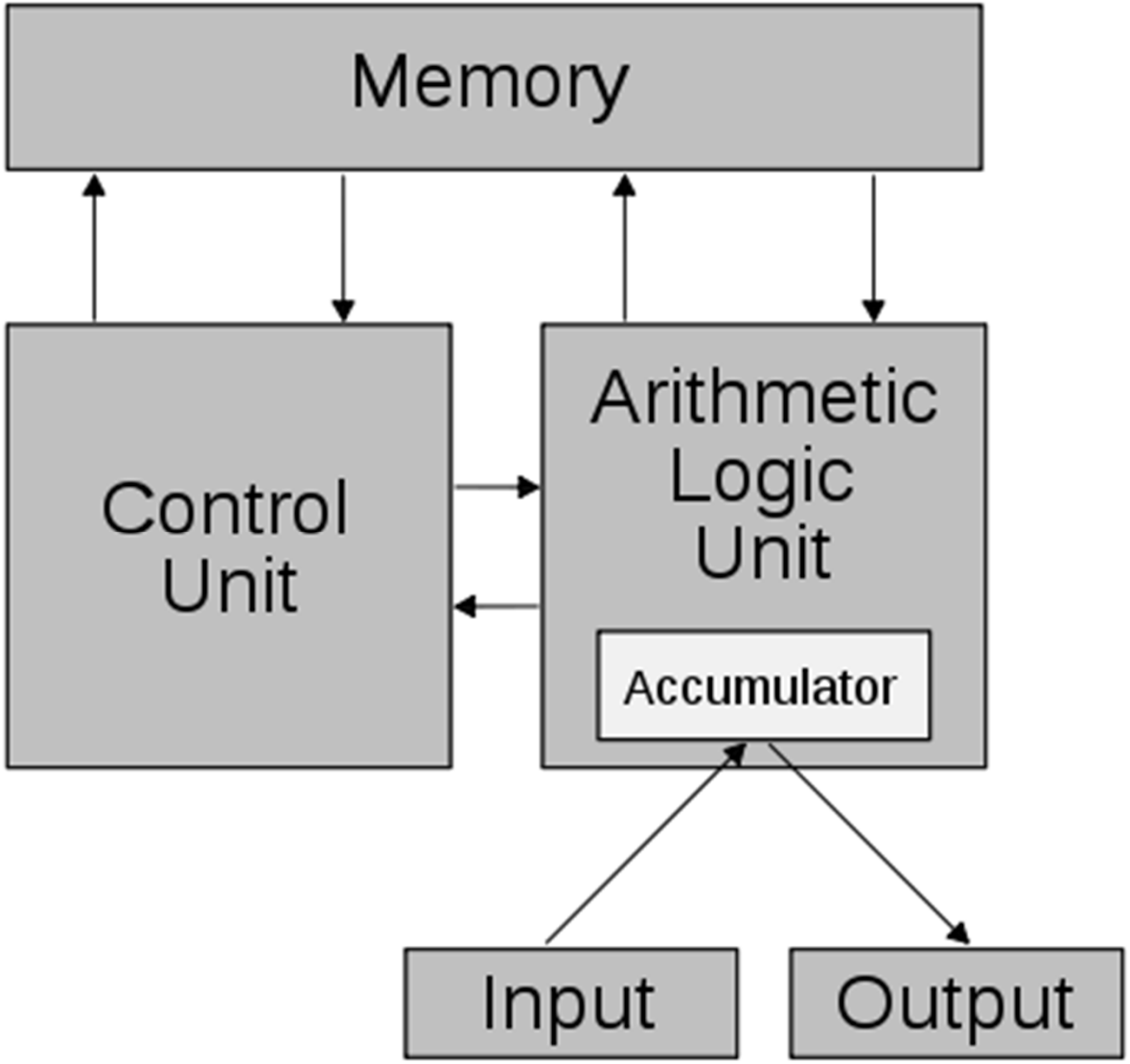
- Review of the first session
- A tour of silicon world!
- Basic definition of CPU
- Von Neumann Architecture
  - Example: Basic ARM7 Architecture
  - A brief detailed explanation of ARM7 Architecture
- Hardvard Architecture
  - Example: TMS320C25 DSP

Agenda (2)

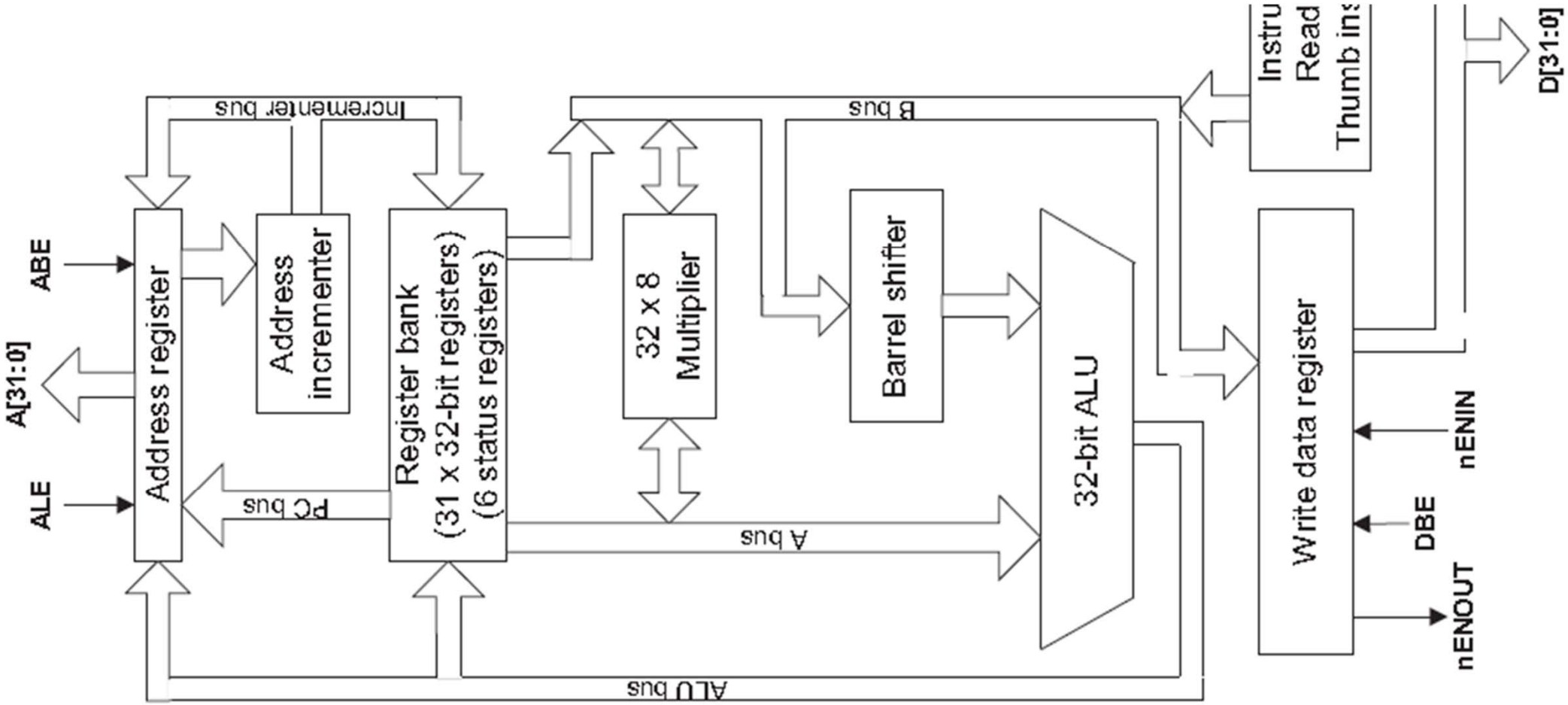
- History of CPUs
  - 4004
  - TMS1000
  - 8080
  - Z80
  - Am2901
  - 8051
  - PIC16

Von Neumann Architecture

- Same Memory
  - Program
  - Data
- Single Bus

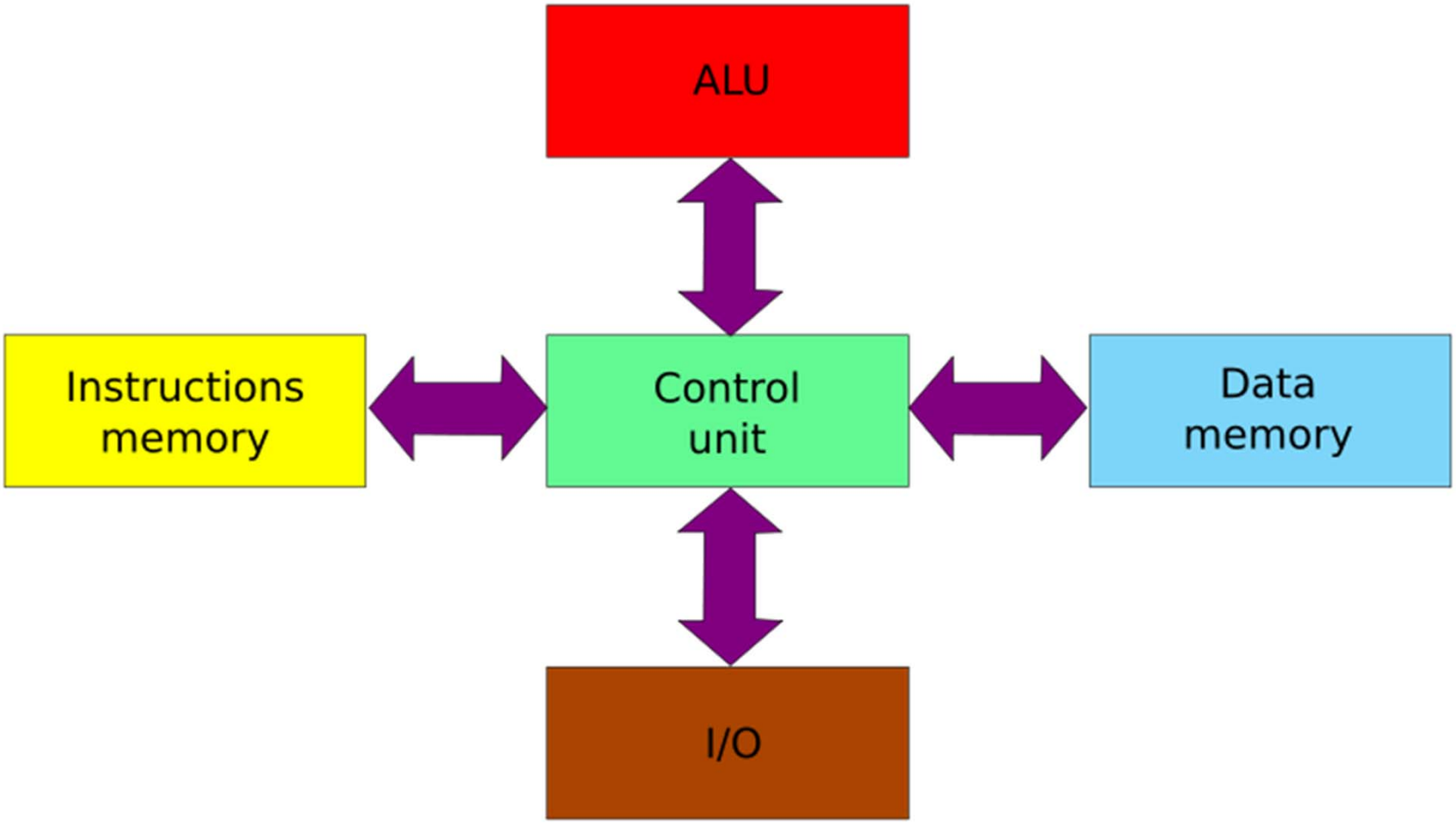


Sample : ARM7T CPU

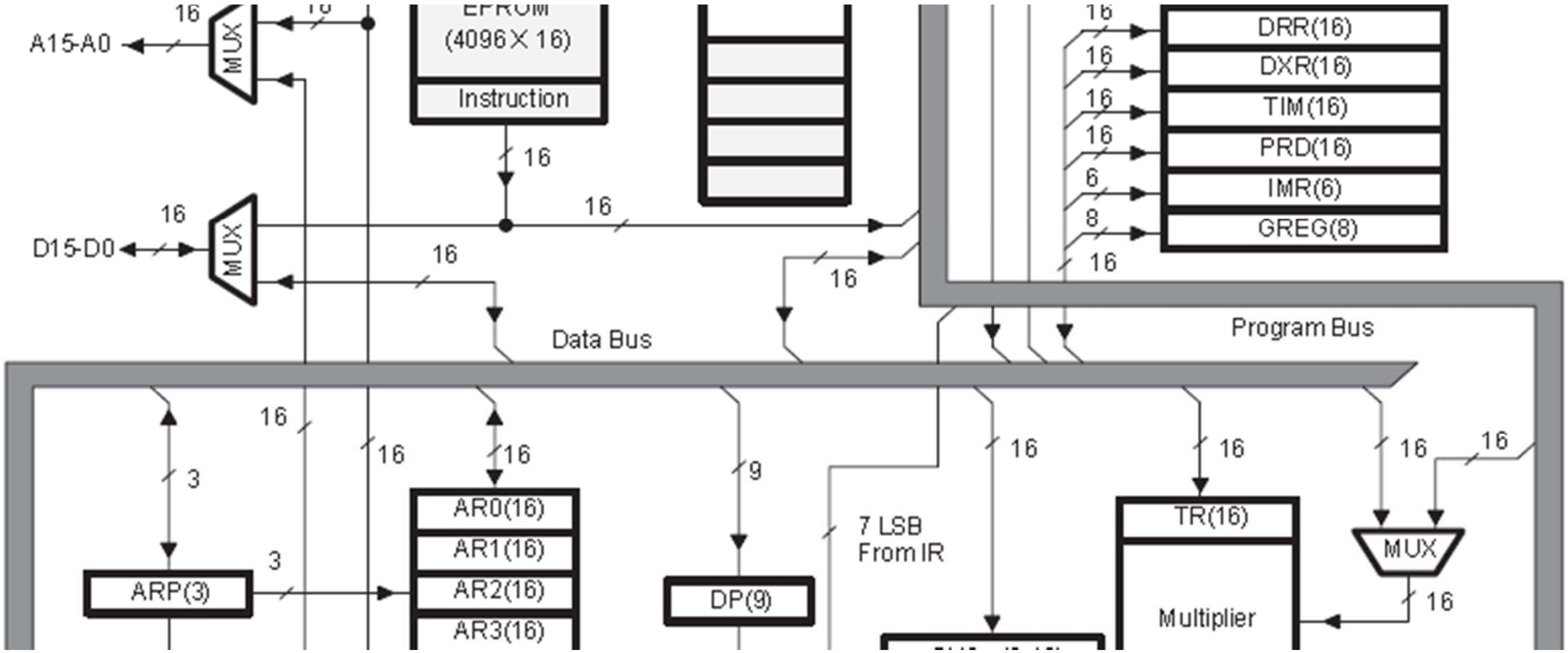


Harvard Architecture

- Separate memories for program and data



TMS320C25 DSP



Silicon Market

Rank 2009	Rank 2008	Company	Country of origin	Revenue (million $ USD)	2009/2008 changes	Market share
1	1	Intel Corporation	USA	32 410	-4.0%	14.1%
2	2	Samsung Electronics	South Korea	17 496	+3.5%	7.6%
3	3	Toshiba Semiconductors	Japan	10 319	-6.9%	4.5%
4	4	Texas Instruments	USA	9 617	-12.6%	4.2%
5	5	STMicroelectronics	FranceItaly	8 510	-17.6%	3.7%
6	8	Qualcomm	USA	6 409	-1.1%	2.8%
7	9	Hynix	South Korea	6 246	+3.7%	2.7%
8	12	AMD	USA	5 207	-4.6%	2.3%
9	6	Renesas Technology	Japan	5 153	-26.6%	2.2%
10	7	Sony	Japan	4 468	-35.7%	1.9%

Silicon Market (2)

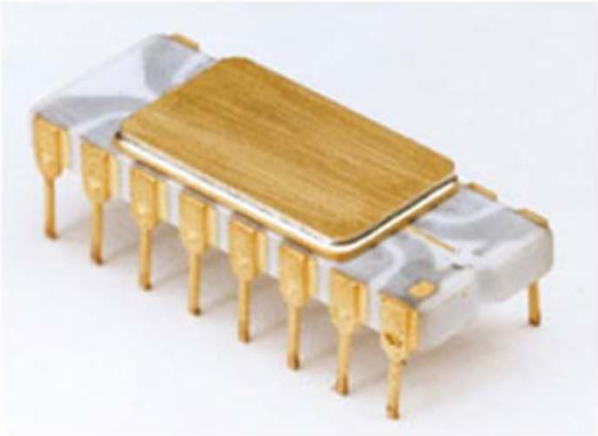
- Total 2009 sales
  - 229,917,000,000 US$
- 2009 sales growth: -11.7%
- Total 2008 sales
  - 258,304,000,000 US$

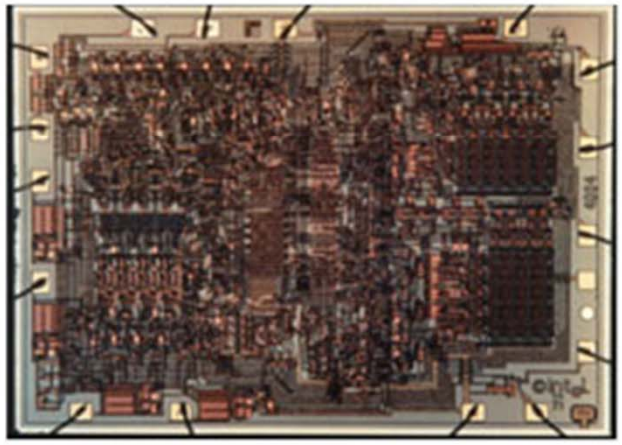
HISTORY

Chapter 2

Intel 4004 (1)

4004 Microprocessor





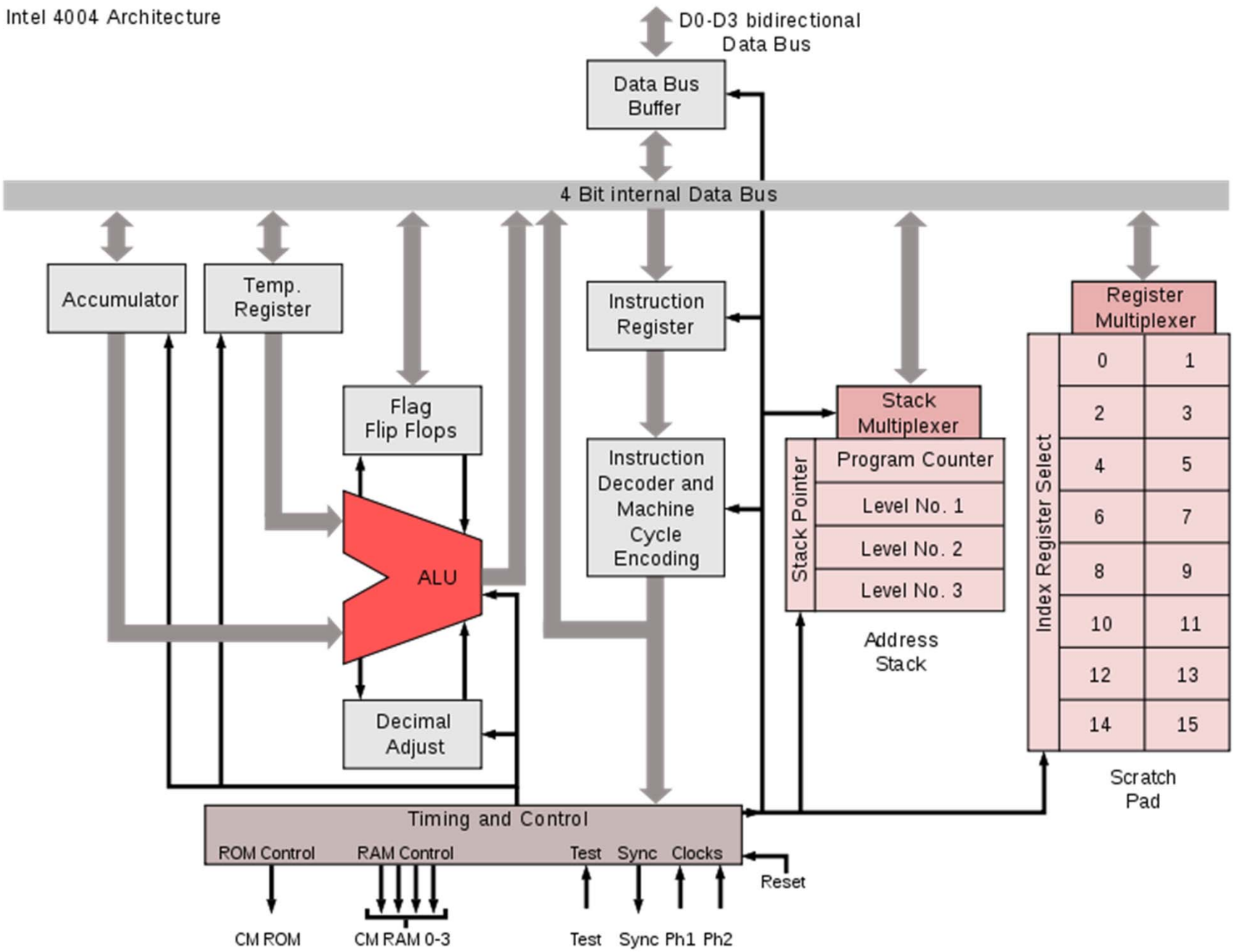
Intel 4004 (2)

- 1971
- Just a calculator (not for industry)
- 4-bits CPU
  - ALU : 4bits
  - Instructions : 8bits
- Separate program and Data memories
  - 1K data memory
  - 4K program memory
    - PC width?

Intel 4004 (3)

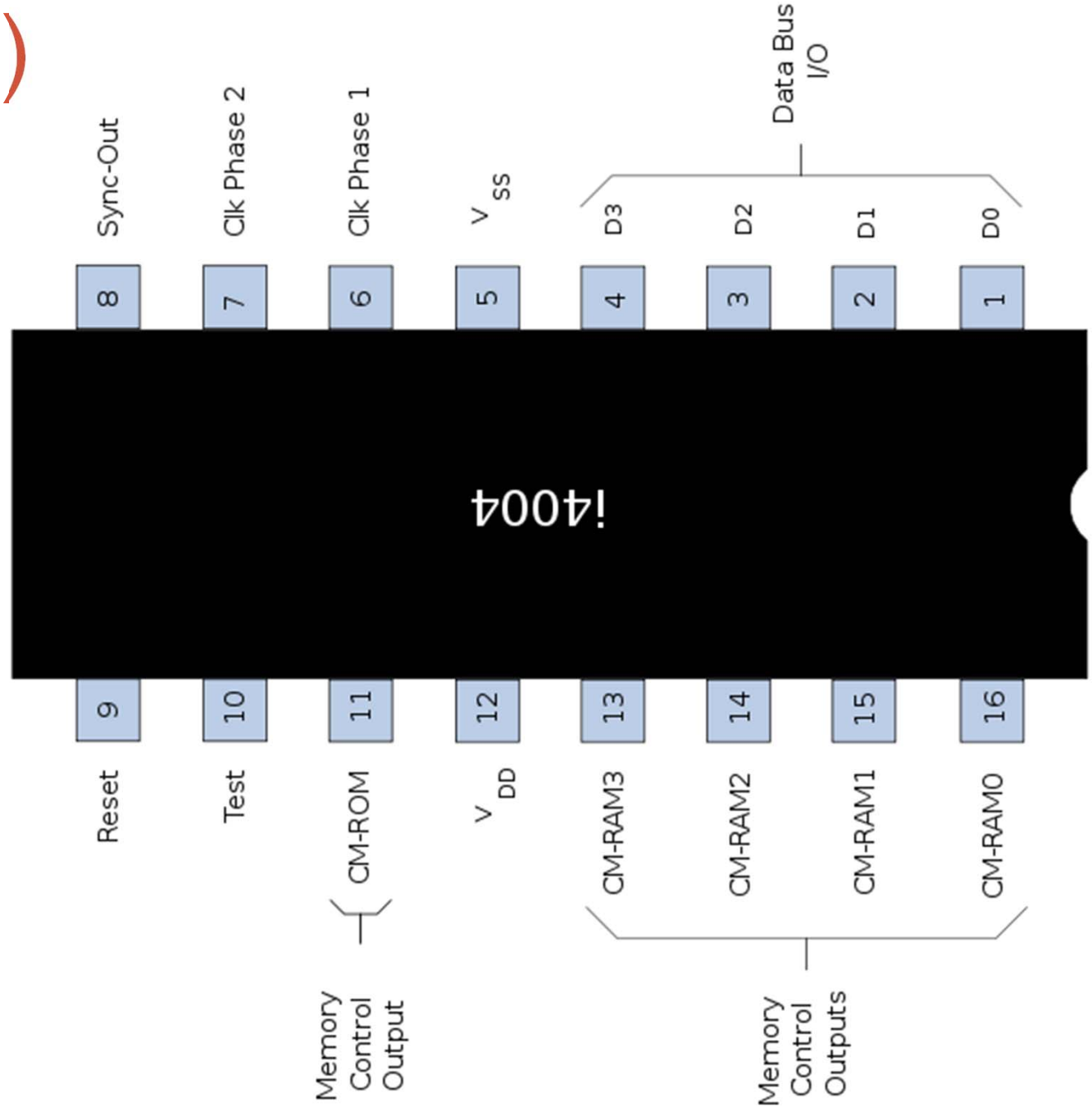
- Registers
  - Sixteen 4 bits registers
- Stack
  - 4 Level stack
- Instructions
  - 46
- Clock frequency : 740kHz
- 2300 transistors
- Speed : 92,000 instructions per second

Intel 4004 (4)


Intel 4004 Architecture
D0-D3 bidirectional Data Bus
Data Bus Buffer
4 Bit internal Data Bus
Accumulator
Temp. Register
Flag Flip Flops
ALU
Decimal Adjust
Instruction Register
Instruction Decoder and Machine Cycle Encoding
Stack Multiplexer
Stack Pointer
Program Counter
Level No. 1
Level No. 2
Level No. 3
Address Stack
Register Multiplexer
Index Register Select
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Scratch Pad
Timing and Control
ROM Control
RAM Control
Test
Sync
Clocks
Reset
CM ROM
CM RAM 0-3
Test
Sync
Ph1
Ph2

Intel 4004 (5)

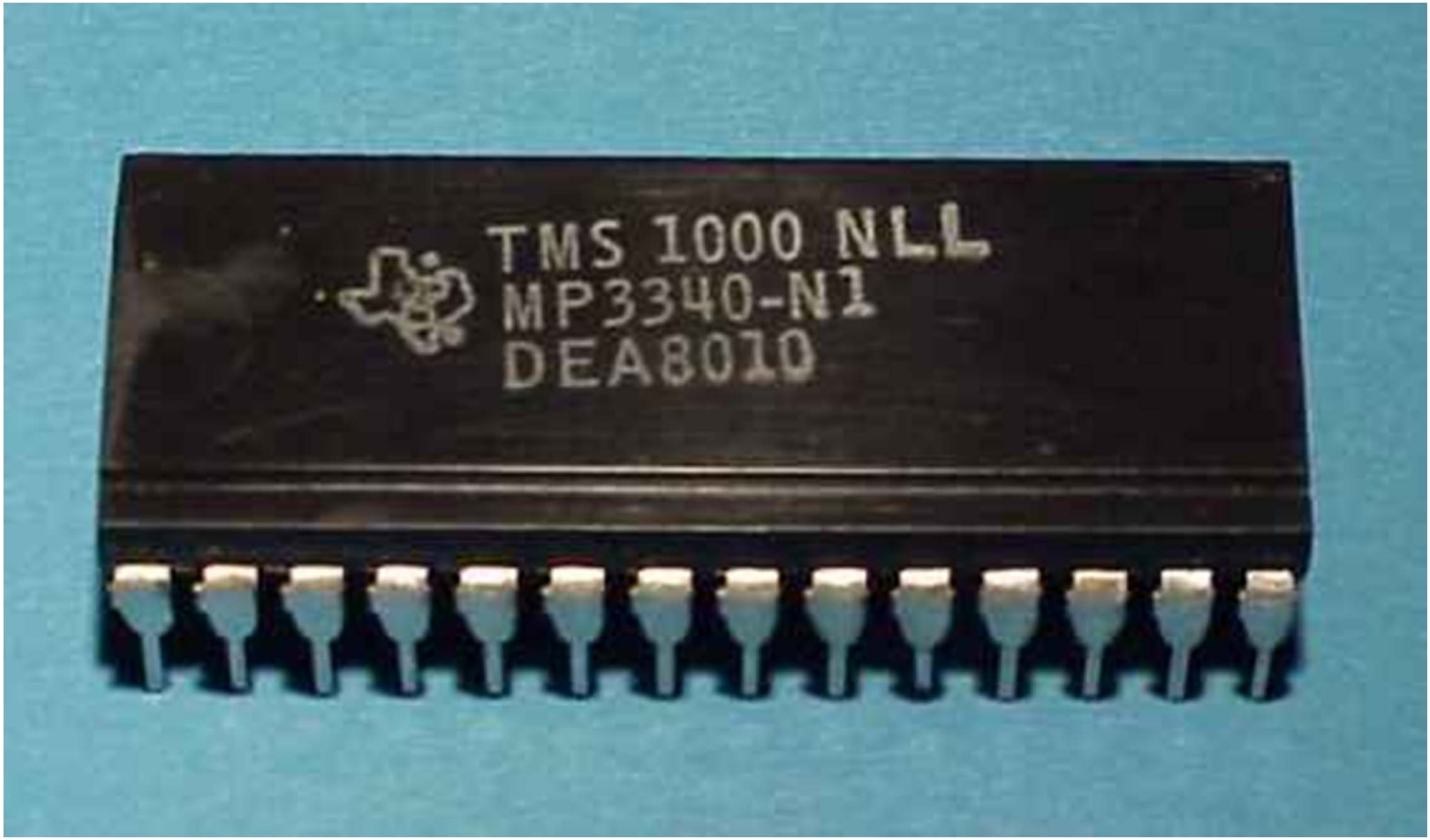
- Single multiplexed 4 bit bus:
  - 12 bit addresses
  - 8 bit instructions
  - 4 bit data



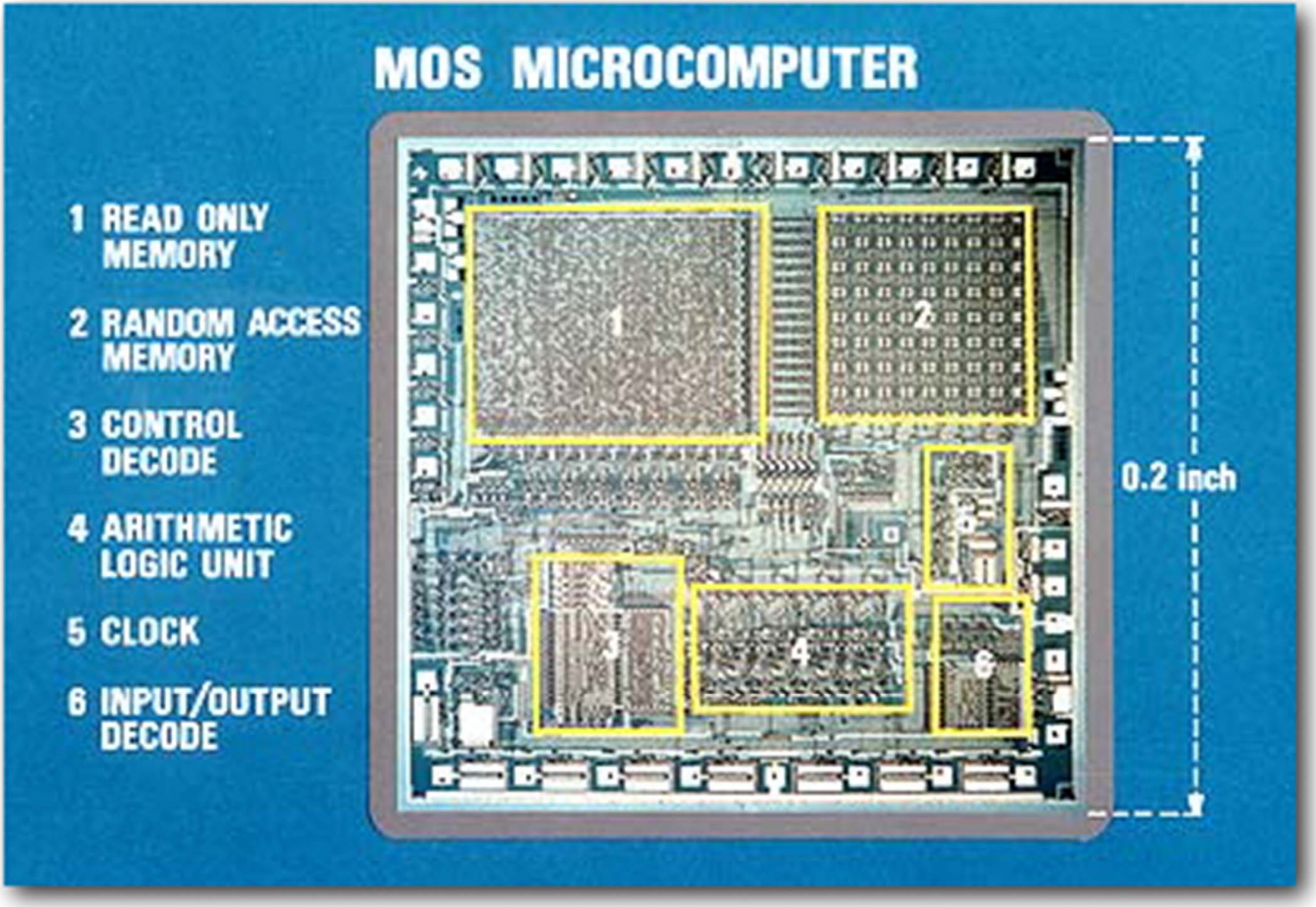
Intel 4004 (6)

- Supported Chips:
  - 4001 : 256Bytes ROM
  - 4002 : 40Bytes RAM
  - 4003 : 10bit shift register
  - 4008 : 8bit address latch
  - 4009 : programmed I/O access
  - 4269 : keyboard , display interface

Texas Instruments TMS1000



Texas Instruments TMS1000 (2)



Texas Instruments TMS1000 (3)

- 1974
- First Micro-controller
  - Computer on a chip
  - MPU, RAM, ROM, Timers
- Clock
  - 300KHz
- Address space
  - 1KB

Texas Instruments TMS1000 (4)

- RAM
  - 32 Bytes
- ROM
  - 1KBytes
- Instructions
  - 31
- Registers : different size each!
- PC : not a counters, but a shift register!

Intel 8080

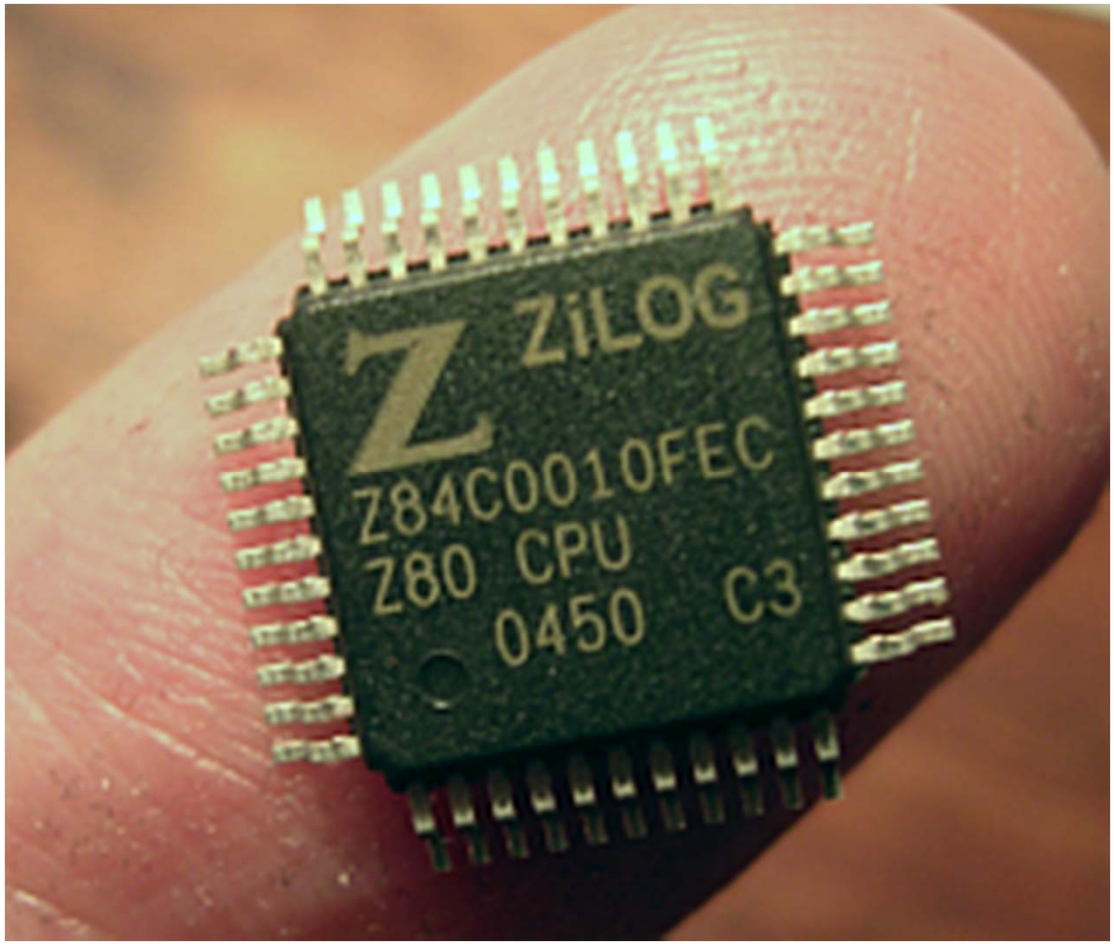
- 1974
- 8bits CPU
- Buses
  - 16bits address bus
    - What range?
    - 16bits PC
    - 16bits Stack Pointer
  - 8bits data bus
- 7 registers : 8bits each

Intel 8080 (2)

- Some registers could join to make 16bits registers
- Separate
  - Memory port
    - To talk to external memory
  - I/O port
    - To talk to external peripherals and devices
- Update : 8085 (1976)
  - Added interrupt pins and serial I/O pins

Zilog Z80

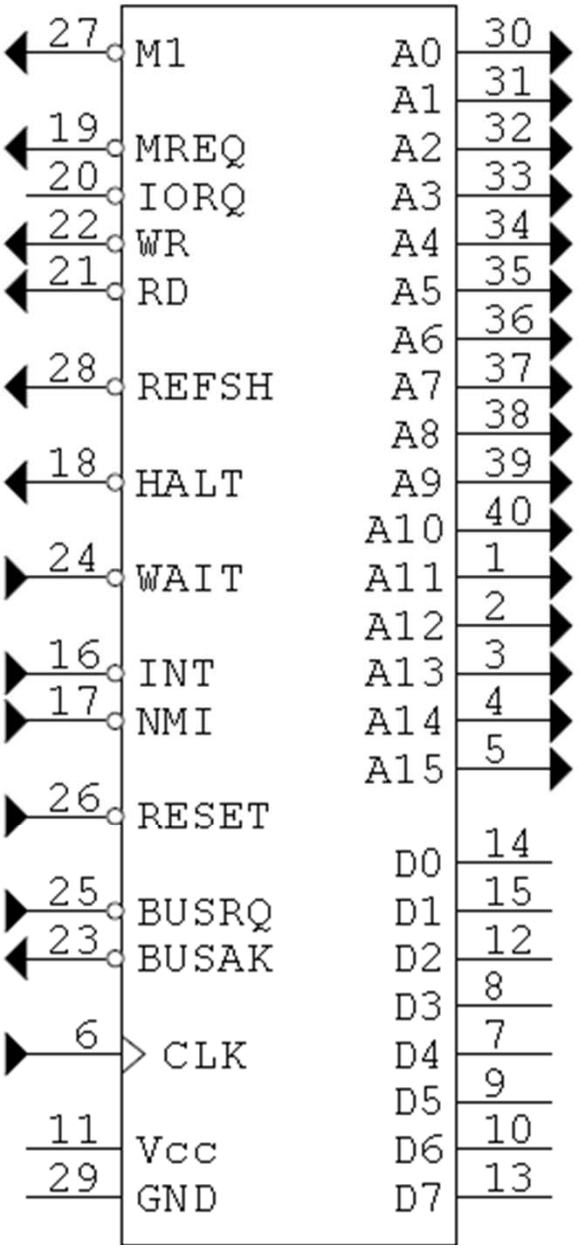
- 1976
- An improved 8080
  - 80 additional instructions
    - Block move instructions
    - Bit manipulation
  - 2 Register banks
    - Suitable for interrupt handling
- Federico Faggin
  - Left Intel at 1974
  - After his work on 8080
  - Founded Zilog

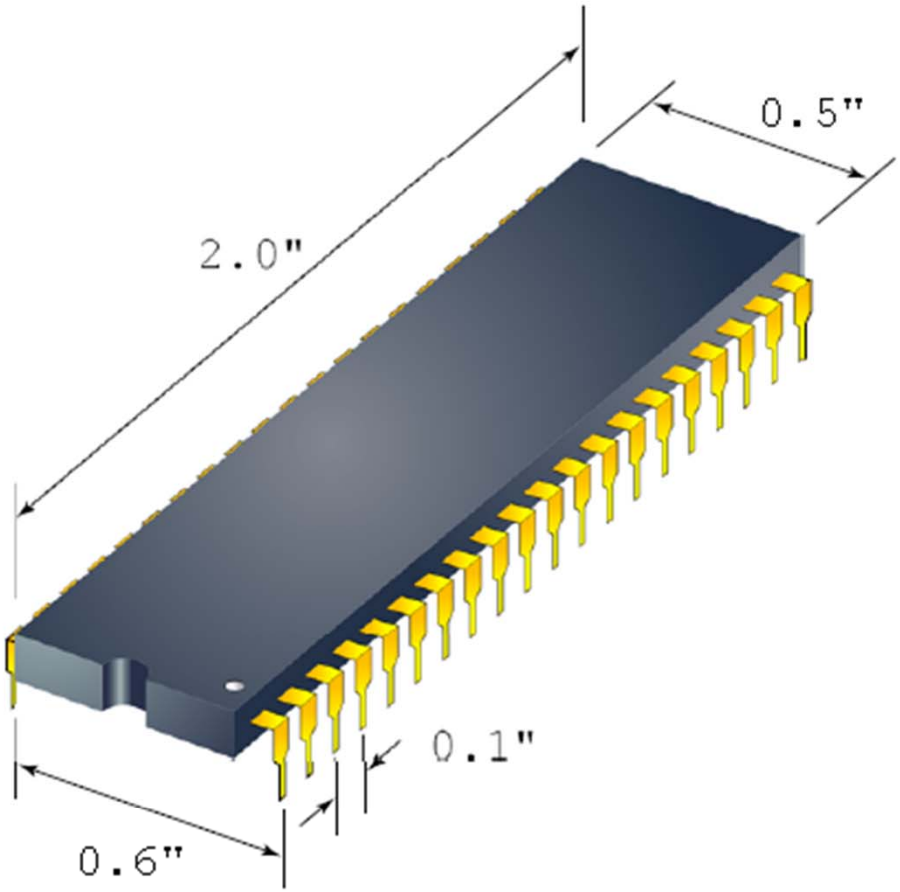


Zilog Z80 (2)

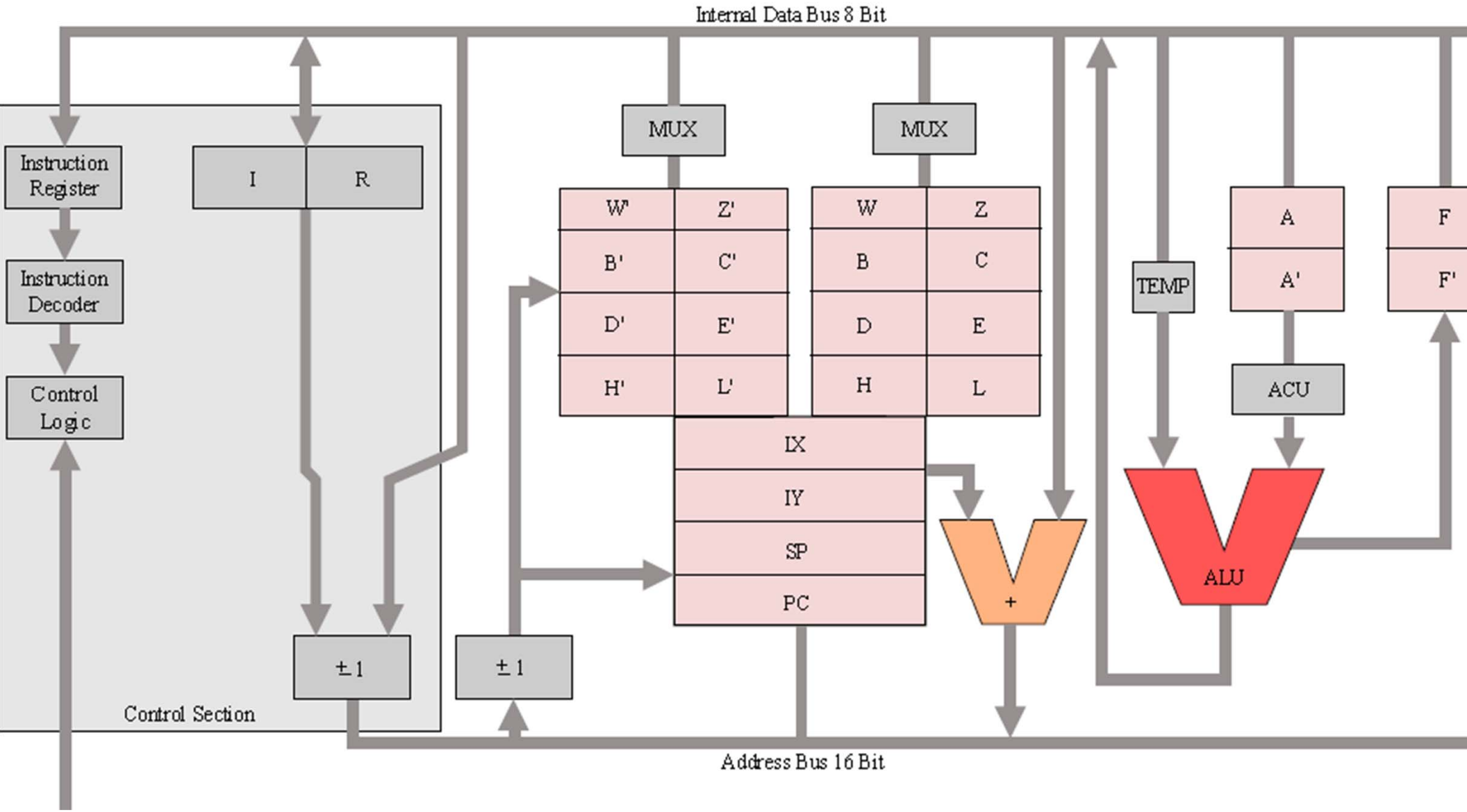
- Clock Frequency:
  - 2.5MHz to 20 MHz (NMOS to CMOS)
- Memory interface
  - Z80 capable of generating DRAM refresh signals itself
- CP/M
  - Fist operating system for microprocessors
  - Mainly designed for 8080
  - Z80 and 8080 were code compatible
- Extensions to Z-80
  - Z180, Z280, Z800
  - eZ80 : 24bits core

Zilog Z80 (3)


27 M1
19 MREQ
20 IORQ
22 WR
21 RD
28 REFSH
18 HALT
24 WAIT
16 INT
17 NMI
26 RESET
25 BUSRQ
23 BUSAK
6 CLK
11 Vcc
29 GND
A0 30
A1 31
A2 32
A3 33
A4 34
A5 35
A6 36
A7 37
A8 38
A9 39
A10 40
A11 1
A12 2
A13 3
A14 4
A15 5
D0 14
D1 15
D2 12
D3 8
D4 7
D5 9
D6 10
D7 13


0.5"
2.0"
0.1"
0.6"

Zilog Z80 (4)


Internal Data Bus 8 Bit
Instruction Register
Instruction Decoder
Control Logic
I
R
±1
Control Section
MUX
MUX
W'
Z'
B'
C'
D'
E'
H'
L'
W
Z
B
C
D
E
H
L
IX
IY
SP
PC
±1
+
TEMP
A
A'
ACU
ALU
F
F'
Address Bus 16 Bit

Zilog Z80 (5)

- Registers
  - A : Accumulator
  - F : Flags
    - Carry, Zero, Parity, …
  - BC, DE, HL : 8/16bits registers
    - 8bits for computations
    - 16bits for address generation
  - SP : 16bits stack pointer
  - PC : 16bits program counter
  - IX , IY : 16bit index register
  - R : 8bits DRAM refresh counter
  - I : 8bits interrupt vector, base register
- Shadow registers : AF’, BC’, DE’, HL’

Zilog Z80 (6)

- Addressing modes:
  - Immediate:
    - LD A,FFH
    - LD HL,1234H
  - Page zero (used for jumps and calls)
  - Relative (used for jumps and calls)
  - Extended addressing (used for jumps and calls)
  - Indexed addressing
    - LD A,(IX+1)
    - LD A,(IY-4)
  - Register indirect addressing
    - LD A,(HL)

Zilog Z80 (7)

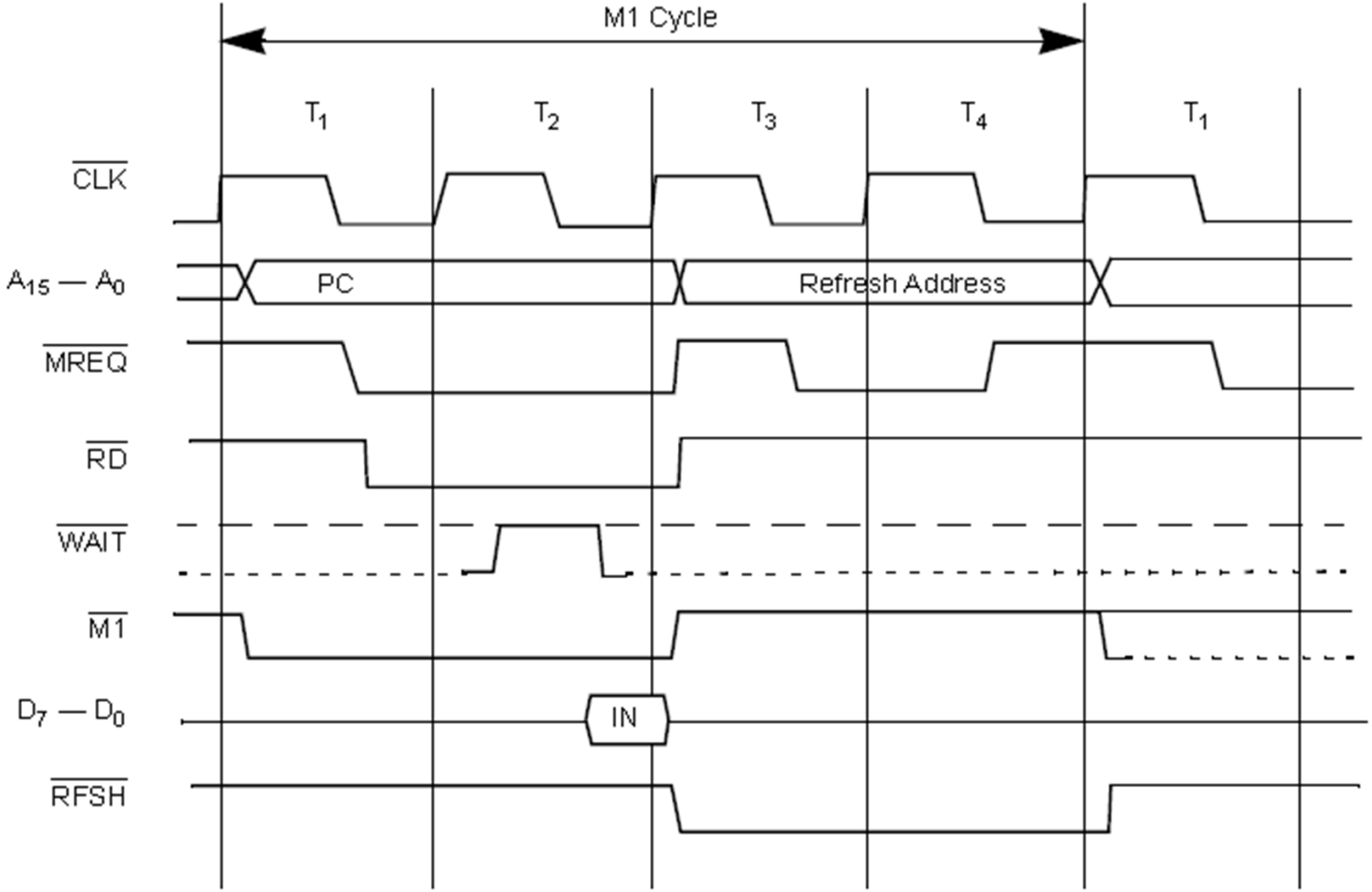
The assembly program:

```
ORG 100H            ;Locate program at 100H
LD   HL,1234H       ;Address of first number
LD   A,(HL)         ;Operand 1 into Accu
INC  HL             ;Address of 2nd number
ADD  A,(HL)         ;Addition
INC  HL             ;Address of result (sum)
LD   (HL), A        ;store result
END                 ;end of program

ORG 1234H           ;Location of the data
DB 100,200          ;put 64H and C8H
```

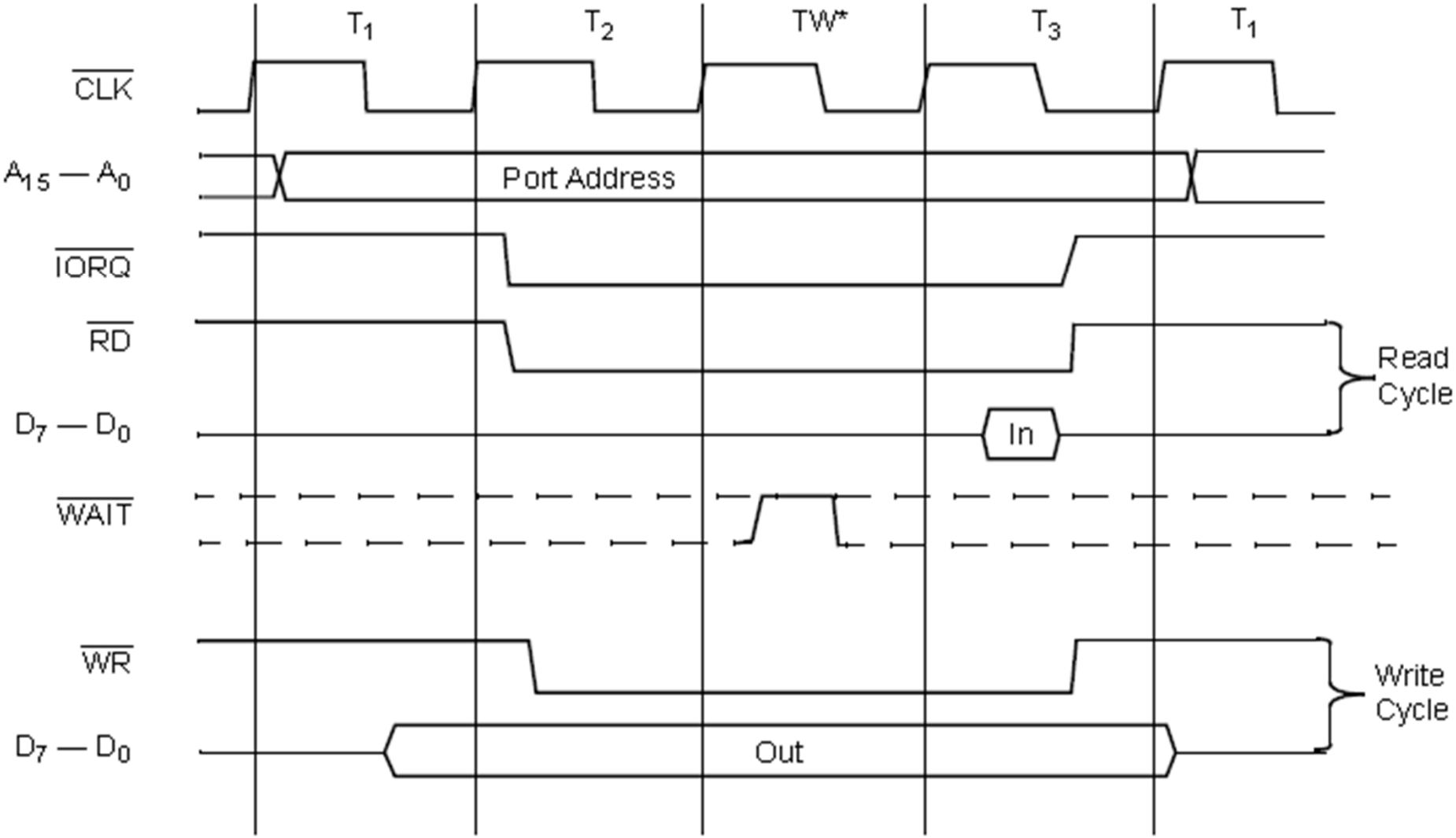
Zilog Z80 (8)

- Instruction: LD A,(HL)



Zilog Z80 (9)

- Instruction : OUT n,A



AMD AM2901

- 4bits CPU
  - 4-bit-slice processor
- Contained ALU and control signals
  - 8bit ALU consists of two 4bits ALU
- 16 registers 4bits each
- AM2903 : contained multiply operation
- AMD9511 : First floating point coprocessor
  - 1979
  - 32bits operations

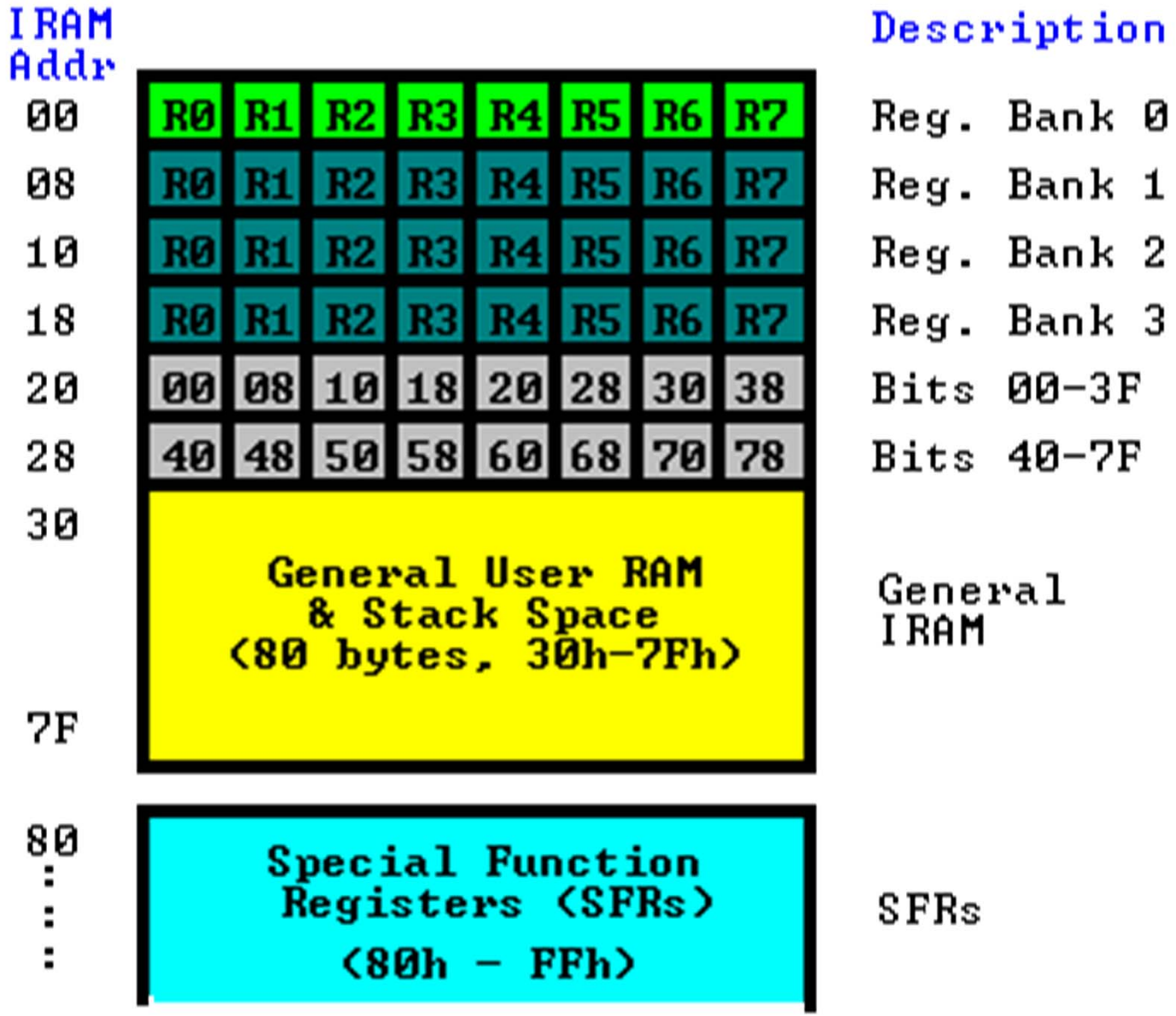
Intel MCS-51

- 1977
- Microcontroller
  - On-chip RAM and ROM
- 2bytes instruction set
- Over 1Billion sold from 1988
- Extensions by Siemens and TI
- Available widely today
  - In different forms

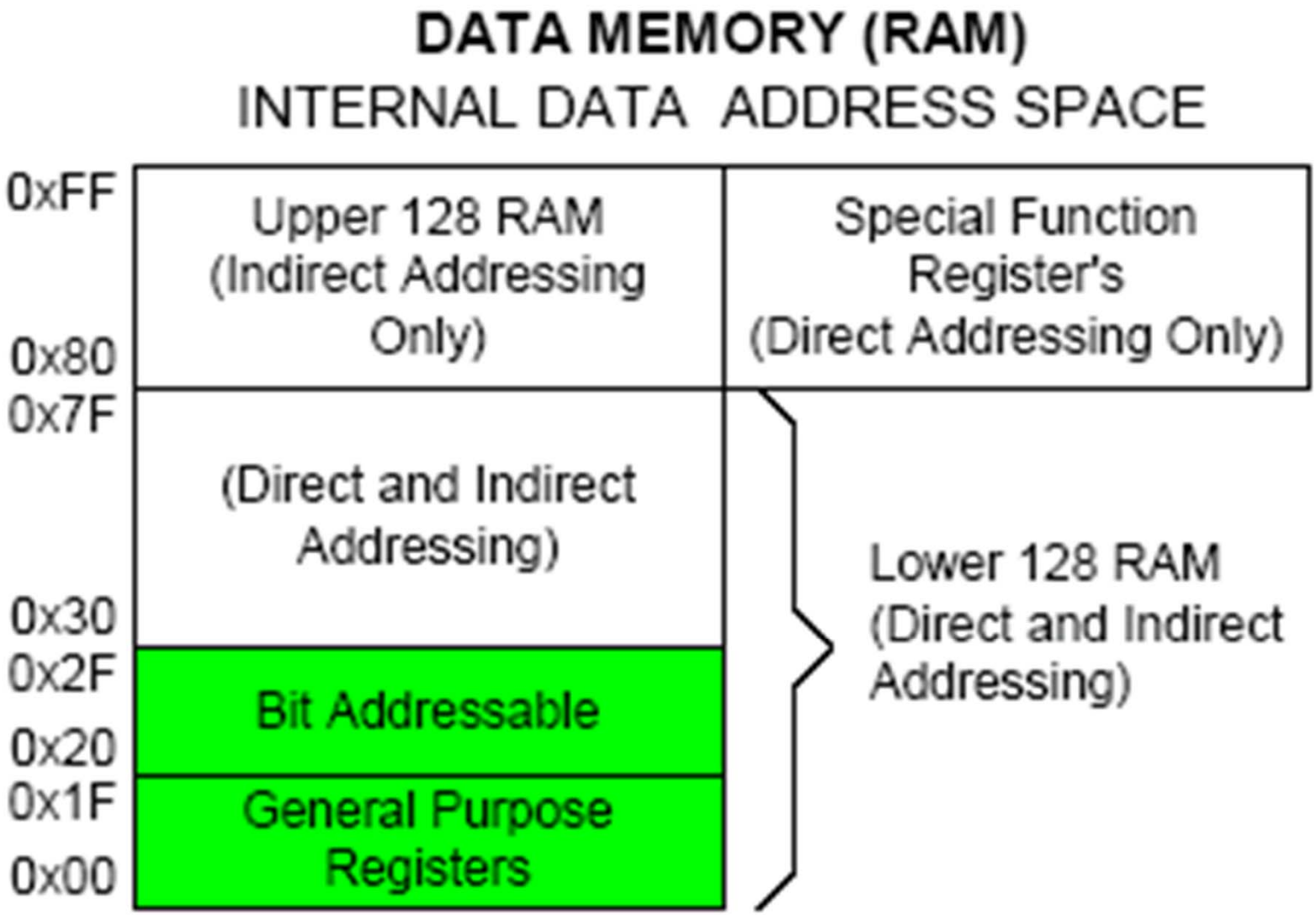
Intel MCS-51 (2)

- Four separate register sets
- Internal static RAM:
  - 80C51 : 128 Bytes
  - 80C52 : 256 Bytes
  - Address Range : 0x0 – 0xff
    - 0x0 – 0x7f : can be accessed directly (128bytes)
      - Example : `MOV A,30h`
    - 0x7f – 0xff : should be accessed indirectly
      - Example : `MOV A,@R0`
    - 0x7f – 0xff : Are control registers of 8051 (Special Function Registers)
    - 0x20 – 0x2f : bit accessible
- Internal program memory
- Support for external memory

MCS-51 Internal Memory



MCS-51 Internal Memory



MCS-51 Bit Memory

- Addresses : 20H – 30H
- Bit Address: 00H – 7FH (128bits total)
- Instruction sample:
  - SETB 24H
  - CLR 25H
  - MOV 20H,#0FFH
    - Equivalent to 8 SETB operations
- Bit Address: 80H – FFH
  - Used for accessing SFR
  - Example:
    - MOV P0,#01
    - SETB 80H

MCS-51 (3)

- Supported Peripherals
  - UART
    - universal asynchronous receiver transmitter
    - Serial interface (TX/RX)
  - Timers
    - time measurement
    - Make an event happen in a specified intervals
  - I2C
    - inter-integrated circuit bus
    - Multi-master bus
    - Mainly to transfer control data
  - SPI
    - Serial peripheral interconnect
    - Serial data transfer for memories

MCS-51 (4)

- Supported peripherals (2)
  - USB
    - Peripheral
    - Host
- CAN
  - Controller-area network
  - A bus to allow microcontrollers talk to each other in a vehicle
  - Without a host computer
  - Now also used in industrial automation and medical equipment
- PWM generator
  - Generate PWM pulses

MCS-51 (5)

- Supported Peripherals
  - Analog comparator
  - A/D and D/A
  - RTC
    - A computer clock
    - Keeps track of the current time
    - Keeps accurate time and date

MCS-51 Special Function Registers

80	P0	SP	DPL	DPH				PCON	87
88	TCON	TMOD	TL0	TL1	TH0	TH1			8F
90	P1								97
98	SCON	SBUF							9F
A0	P2								A7
A8	IE								AF
B0	P3								B7
B8	IP								B9
C0									C7
C8									CF
D0	PSW								D7
D8									DF
E0	ACC								E7
E8									EF
F0	B								F7
F8									FF

Blue background are I/O port SFRs
Yellow background are control SFRs
Green background are other SFRs

MCS-51 Ports

- 8051/52 has 4 ports
  - General purpose I/O
  - P0, P1, P2, P3
- Using external memory:
  - Program is stored outside 8051
  - P0 & P2 will be used for memory interfacing

MCS-51 Stack Pointer

- SP points to the tail of the stack
- PUSH A
  - SP ← SP+1
  - Value A will be stored in memory address : SP
- POP A
  - Value A will be read from memory address : SP
  - SP ← SP – 1
- Instructions that change SP:
  - CALL, RET, POP , PUSH, interrupts

MCS-51 SFRs

- DPL/DPH : DPTR , Data pointer
  - 16bits register
  - Used for addressing external operands
- PCON : Power control
  - Sleep mode
- TCON :Timer control
  - Stop, start , overflow…
- TMOD : Timer mode
  - 16bits timers/13bits/ two separate 8bits
  - Count what? Events? External pin changes?
- TL0/TH0 , TL1/TH1 : Timers
  - Always count up

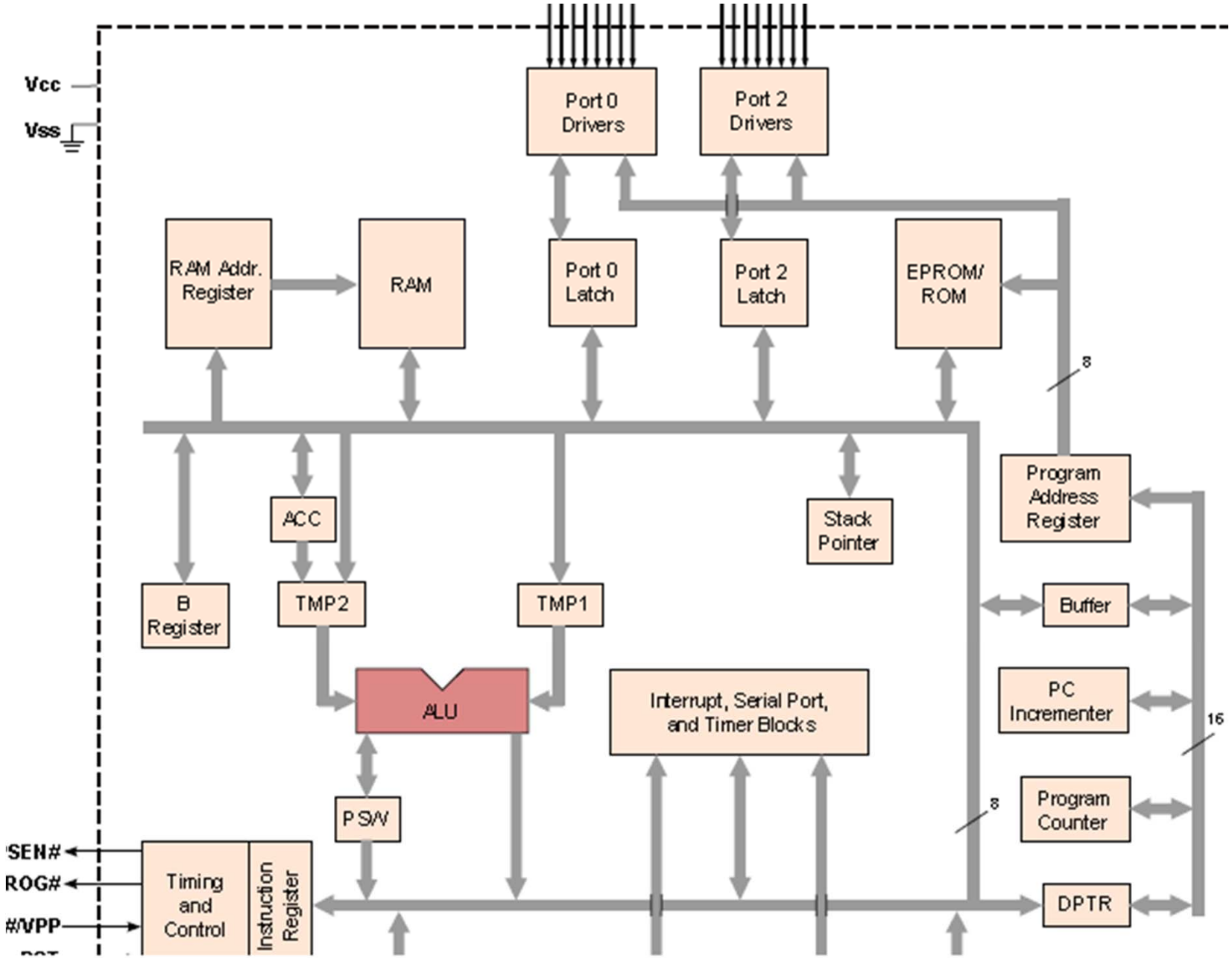
MCS-51 SFRs (2)

- SCON: serial control
  - Baud rate
  - Start/stop
  - Flags
- SBUF : serial port data buffer
- IE : Interrupt enable
- IP : interrupt priority
  - Example: High priority for serial interrupt
- PSW : program status word
  - Carry flag, overflow flag, parity flag,…
  - Register bank select bits
- ACC : Accumulator
  - MOV E0H,#20h == MOV A,#20h
- B : used for divide and multiply operations

MCS-51 Addressing Modes

- Immediate addressing
  - MOV A,#20h
- Direct Addressing
  - MOV A,30h
- Indirect Addressing
  - MOV A,@R0
- External Addressing
  - MOVX A,@DPTR
- Code Indirect
  - MOVC A,@DPTR

Intel MCS-51


Vcc
Vss
Port 0 Drivers
Port 2 Drivers
RAM Addr. Register
RAM
Port 0 Latch
Port 2 Latch
EPROM/ ROM
8
Program Address Register
ACC
Stack Pointer
B Register
TMP2
TMP1
Buffer
ALU
Interrupt, Serial Port, and Timer Blocks
PC Incrementer
16
PSW
8
Program Counter
SEN#
ROG#
#VPP
Timing and Control
Instruction Register
DPTR

Microchip Corporation

- Created 1987
  - A “General Instrument” company spin off
- Products
  - Micro-controllers
    - PIC16/18
    - PIC24/32
    - dsPIC
    - Serial storage :
      - Serial EEPROM
      - Serial SRAM
  - USB controllers
  - ZigBee interfaces

Microchip PIC

- 1975
- PIC : Programmable Interface Controller
- Designed in Harvard University
  - To be used in a commercial product
  - In “General Instrument” company
- A new company born
  - Arizona Microchip Technology
- 2008:
  - Microchip announced its six billionth PIC processor shipment

PIC Micro-controllers

- No difference between
  - Memory space
  - Register space
  - RAM serves as: memory & registers
- Banking mechanism
  - Extend addressing range
  - Data transfers should happen within a bank
    - Or accumulator should be used as temporary storage
  - Later versions
    - Move instructions
    - Capable of addressing whole memory range
- Generally
  - No external memory interface
  - Exception : PIC17 & high pin count PIC18
- Shadow registers in PIC18 for interrupts

Code Space

- ROM
- EPROM
- Flash ROM
- Addressing in program memory:
  - Is not based on Bytes
  - Depends on length of instructions
  - For example:
    - Each memory cell is 12Bits
    - There are total number of 128cells of 12Bits each
    - Example : 4096*14bits for 16F690
- Stack
  - Is not accessible from software
- PIC18
  - Byte addressable memory
  - Software based stack

PIC Performance

- Each instruction
  - Takes 2 instruction cycle to execute
- Execution time
  - Number of instructions * 2
- Interrupt latency is constant
  - 3 instruction cycles
- Measuring performance of a portion of code:
  - Profiling

Real-time system

- A system
  - Which should produce response to input
  - In a specified amount of time
- Profiling
  - Important in making real-time systems
- A program that performs profiling:
  - Profiler
- Every CPU architecture
  - Has its own profiler
- Example:
  - Intel VTune Performance Analyzer

PIC Compilers

- C compiler
- 2008
  - Microchip announced their own compiler
  - For 18F, 24F and 30F devices
- In contrast
  - Atmel AVR
    - Supported by GNU C compiler

PIC10 & PIC16

- PIC16x
  - 33 fixed length 12bits instructions (RISC)
  - 32Bytes register file
  - 2 level deep call stack
  - First 7 to 9 bytes of register file: special purpose registers
  - Bank number : higher 3bits of FSR
  - Registers 0-15 are global
    - Not affected by bank select bits
  - Registers 16-31
    - Will change by bank select bits

Microchip PIC17/18

- PIC17x
  - 16Bits op-codes
  - 16 level deep call stack
  - Read access to code memory
  - Direct register to register moves
  - External program memory interface
  - Single-cycle 8bits multiply
  - 64K-word program space (2K to 8K on chip)
- PIC18x
  - We will have a close look later

dsPIC and PIC24

- 16bits micro-controllers
- Mass production: 2004
- dsPIC : digital signal processing capabilities
- Features
  - Added 16 registers
  - Stack in RAM
  - Direct access to data in program memory
  - Interrupt sources may be assigned to handlers
    - Interrupt vector table

dsPIC

- Supported by : GNU C compiler
- Support for
  - Hardware MAC
    - Single cycle 16X16 multiplication
  - Barrel shifter
  - Direct Memory Access operations

- We will talk about capabilities of DSP chips in depth later!

PIC32

- 2007
- Based on MIPS32 M4K Core
- Supported by GCC
- …

Intel 80x86

- 1978
- 16Bits CPU
- 1979 : Intel 8088
  - The same architecture as 8086
  - 8Bits data bus instead of 16Bits bus
  - Used in first IBM PC
- Clock frequency: 5 – 10MHz

At the time of 8086

- Intel 8085 (1977)
- Motorola 6800 (1974)
- Microchip PIC16X (1975)
- MOS Technology 6502 (1975)
- Zilog Z80 (1976)
- Motorola 6809 (1978)

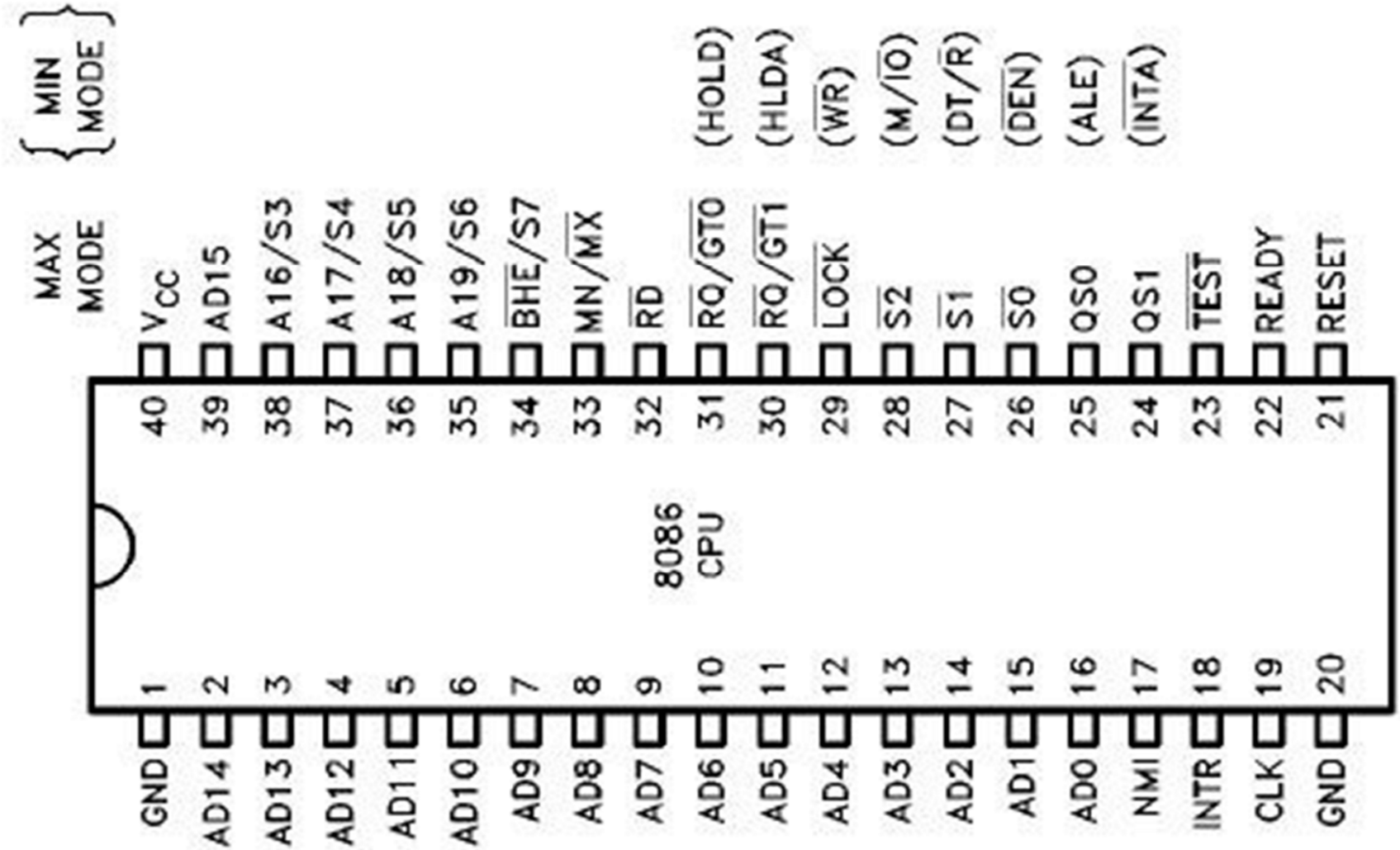
8086

- Project: Spring 1976 – Summer 1978
- Backward compatible
  - 8008, 8080, 8085
- Support for
  - Full 16Bits processing
- Base + Offset addressing
- Self repeating operations
- Micro-coded Multiply & Divide
- Bus structure adapted to co-processors
  - 8087 / 8089

Area & Naming

- 20,000 transistors
- Naming
  - Used in most of the later CPUs
  - 80286, 80386, 80486, 80586 …

8086 pin out


MIN MODE
MAX MODE
8086 CPU
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
RESET 21
READY 22
TEST 23
QS1 24
QS0 25
S0 26
S1 27
S2 28
LOCK 29
RQ/GT1 30
RQ/GT0 31
RD 32
MN/MX 33
BHE/S7 34
A19/S6 35
A18/S5 36
A17/S4 37
A16/S3 38
AD15 39
VCC 40
(HOLD)
(HLDA)
(WR)
(M/IO)
(DT/R)
(DEN)
(ALE)
(INTA)

8086 Modes

- 8086 Minimum Mode
  - Normal mode of operation
  - One CPU is connected to other peripherals
- 8086 Maximum Mode
  - Used when there are multiple processors in system
  - Bus control signals by 8288 bus controller
- IBM/PC
  - Maximum mode
  - CPU + co-processor

8086 Registers

Main registers		
AH	AL	**AX** (primary accumulator)
BH	BL	**BX** (base, accumulator)
CH	CL	**CX** (counter, accumulator)
DH	DL	**DX** (accumulator, other functions)
Index registers		
SI		**S**ource **I**ndex
DI		**D**estination **I**ndex
BP		**B**ase **P**ointer
SP		**S**tack **P**ointer

8086 Registers

Status register																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	(bit position)
-	-	-	-	O	D	I	T	S	Z	-	A	-	P	-	C	Flags
Segment register																
CS																**C**ode **S**egment
DS																**D**ata **S**egment
ES																**E**xtra**S**egment
SS																**S**tack **S**egment
Instruction pointer																
IP																**I**nstruction **P**ointer

8086 Flags

- O : Overflow
  - Set when MSB is set or cleared
- D : Direction
  - Direction of string operation
- I : interrupt enable
  - Set this, enable maskable interrupts
  - NMI is always active
- T : single step flag
- S : sign
  - Set when MSB of the result is set
- Z : Zero flag
- A : Some kind of carry
- P : Parity flag
  - Set if number of 1 is even
- C : Carry flag
  - Set if carry from MSB , or Borrow to MSB happened

Segmentation

- Registers : 16Bits
- External address bus: 20Bits
- Address generation:
  - Segment Register << 4 + Offset Register
- Could address 1MBytes
- Pointers
  - Near : inside a segment
  - Far : every where!

Memory Models

- Compilers
  - Different memory models for programs
  - To specify default pointer size
- Tiny (max 64kbytes)
- Small (128kbytes)
- Compact (data > 64kbytes)
- Medium (code > 64kbytes)
- Large (code , data > 64kbytes)
- Huge (arrays > 64kbytes)

8086

- Separate Memory and I/O space
  - 64kbyte I/O space
- Multiplexed address and data bus
  - Limited performance
- 256 Interrupts

Co-Processors

- 8086
  - Capable of connecting to co-processor chips
  - Floating point calculations
- 8087
  - Math co-processor
  - 80bit values

Compatible Versions

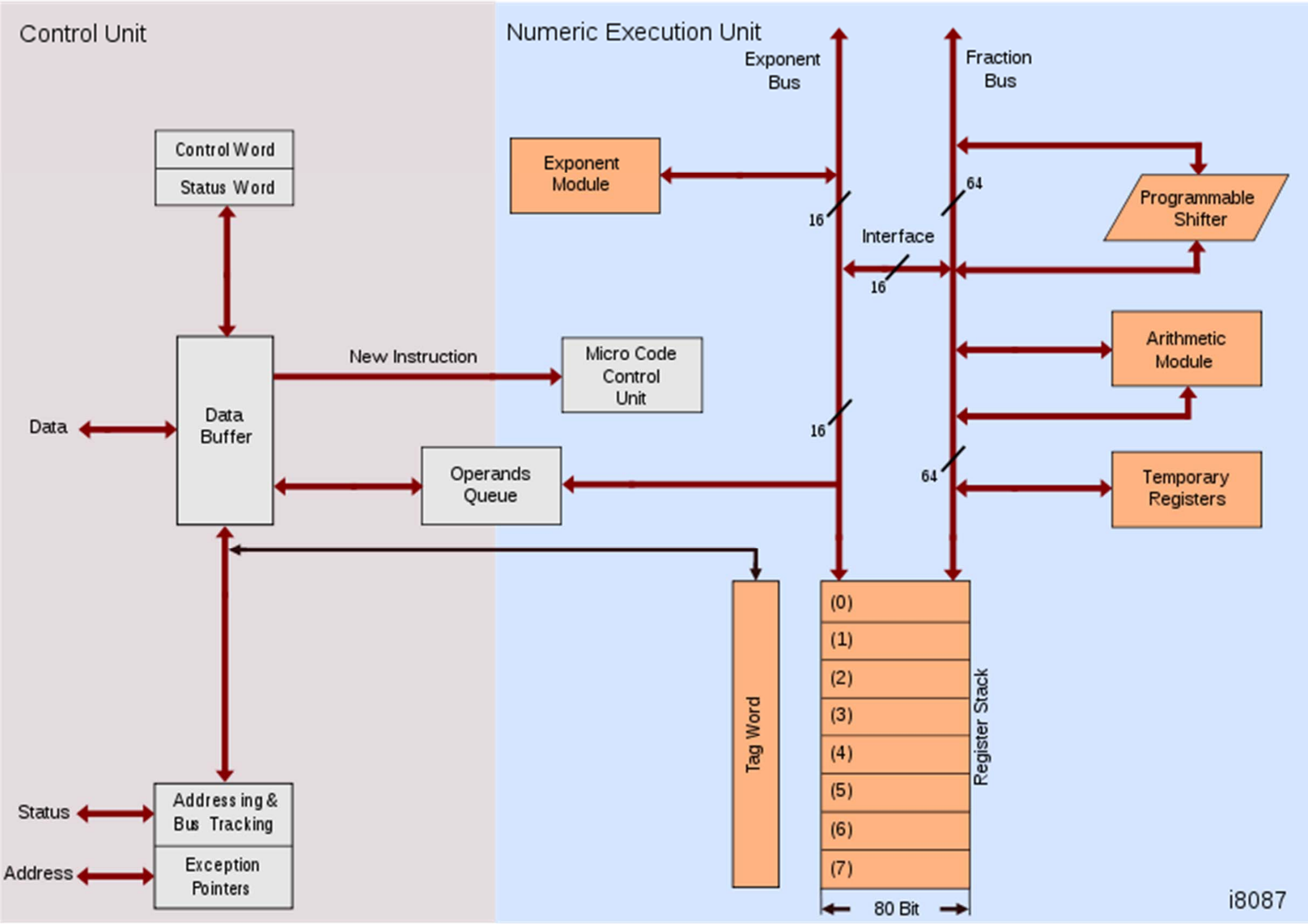
- By
  - Fujitsu
  - Harris/Intersil
  - OKI
  - Siemens
  - Texas Instruments
  - NEC
  - Mitsubishi
  - AMD
  - Soviet Union

Intel 8087

- 1980
- First floating point co-processor for 8086
- 45,000 transistors
- Computation performance
  - 50,000 FLOPS
- 8087 can be paired with 8086, 8088
- All 8087 Assembly instructions begin with
  - FADD, FMUL, FCOM
- All 8087 op-codes begin with
  - 11011 pattern (27 decimal)

Intel 8087

- Registers
  - Not addressable directly
- 8 registers
  - Make a stack
  - 8 levels deep
  - Each register : 80 bits
  - St0 to st7
- Design of 8087
  - Basis of IEEE 754 standard
  - 80387 : first co-processor meeting IEEE standard completely
- Data types in 8087
  - 32/64/80 Bits


Control Unit
Numeric Execution Unit
Exponent Bus
Fraction Bus
Control Word
Status Word
Exponent Module
Programmable Shifter
64
16
Interface
16
Arithmetic Module
New Instruction
Micro Code Control Unit
Data
Data Buffer
16
Operands Queue
64
Temporary Registers
Tag Word
(0)
(1)
(2)
(3)
(4)
(5)
(6)
(7)
Register Stack
Status
Address ing & Bus Tracking
Address
Exception Pointers
80 Bit
i8087

8087 Instruction Execution

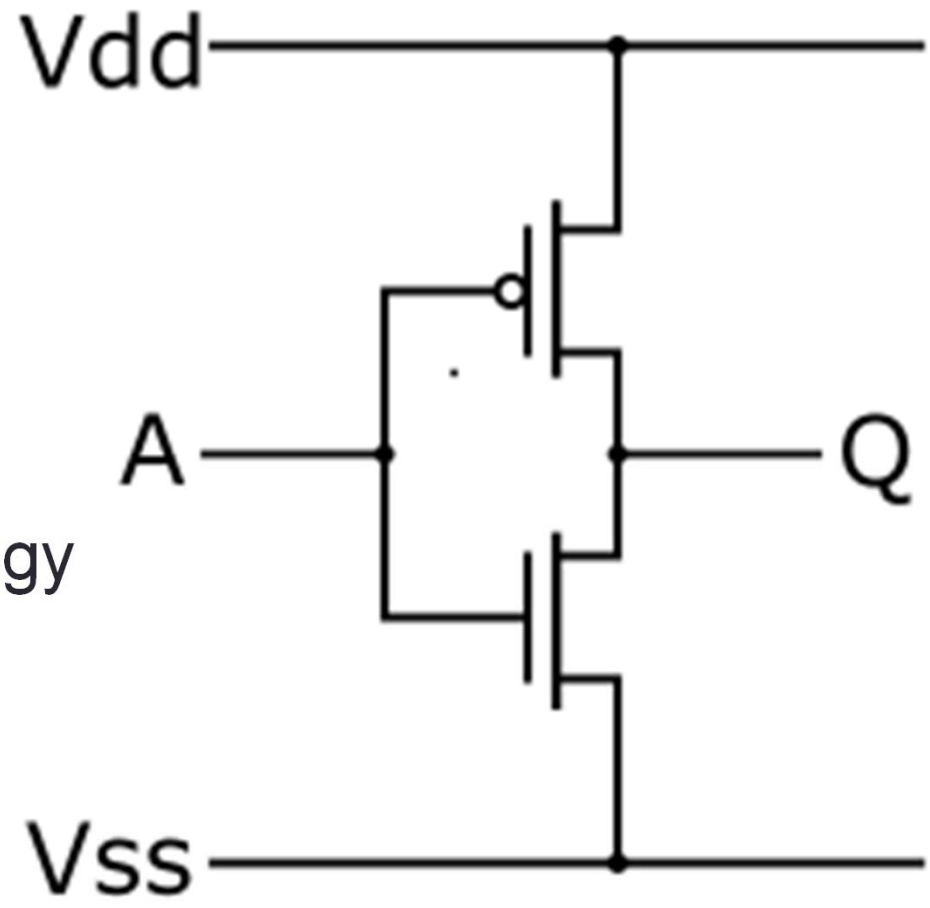
- 8087
  - Directly connected to Data and Address buses of 8086 CPU
- 8086
  - Gives control to 8087
  - When it encounters instructions that begin with 27
  - 8087 gives the control back when finished with operations
- Later co-processors
  - Did not connect to buses directly
  - Instruction was given by CPU itself

A BRIEF LOOK…

CHAPTER 2

Logic Gates

- NOT
  - 2 transistors
- FET switches
  - Built using Silicon
  - Not ideal
- Leakage current
- Manufacturing technology
- Clock frequency



Transistor Count

Function	Transistor count
NOT	2
BUF	4
NAND 2-input	4
XOR 2-input	6
XNOR 2-input	8
NOT MUX 2-input	8
MUX 4-input	24
Adder full	28
Latch, D gated	8
Flip-flop, edge triggered dynamic D with reset	12

CPU transistor count (1)

Processor	Transistor count	Date of introduction	Manufacturer	Process	Area
Intel 4004	2,300	1971	Intel	10 µm	
Intel 8008	3,500	1972	Intel	10 µm	
MOS Technology 6502	3,510	1975	MOS Technology		
Intel 8080	4,500	1974	Intel	6 µm	
Intel 8088	29,000	1979	Intel	3 µm	
Intel 80286	134,000	1982	Intel	1.5 µm	

CPU transistor count (2)

Intel 80386	275,000	1985	Intel	1.5 µm
Intel 80486	1,180,000	1989	Intel	1 µm
Pentium	3,100,000	1993	Intel	0.8 µm
AMD K5	4,300,000	1996	AMD	0.5 µm
Pentium II	7,500,000	1997	Intel	0.35 µm

CPU transistor count (3)

AMD K6	8,800,000	1997	AMD	0.35 µm
Pentium III	9,500,000	1999	Intel	0.25 µm
AMD K6-III	21,300,000	1999	AMD	0.25 µm
AMD K7	22,000,000	1999	AMD	0.25 µm
Pentium 4	42,000,000	2000	Intel	180 nm
Atom	47,000,000	2008	Intel	45 nm
Barton	54,300,000	2003	AMD	130 nm
AMD K8	105,900,000	2003	AMD	130 nm
Itanium 2	220,000,000	2003	Intel	130 nm
Cell	241,000,000	2006	Sony/IBM/Toshiba	90 nm

CPU transistor count (4)

Core 2 Duo	291,000,000	2006	Intel	65 nm	
AMD K10	463,000,000[1]	2007	AMD	65 nm	
AMD K10	758,000,000[2]	2008	AMD	45 nm	
Itanium 2 with 9MB cache	592,000,000	2004	Intel	130 nm	
Core i7 (Quad)	731,000,000	2008	Intel	45 nm	263 mm²
POWER6	789,000,000	2007	IBM	65 nm	341 mm²
Six-Core Opteron 2400	904,000,000	2009	AMD	45 nm	

CPU transistor count (5)

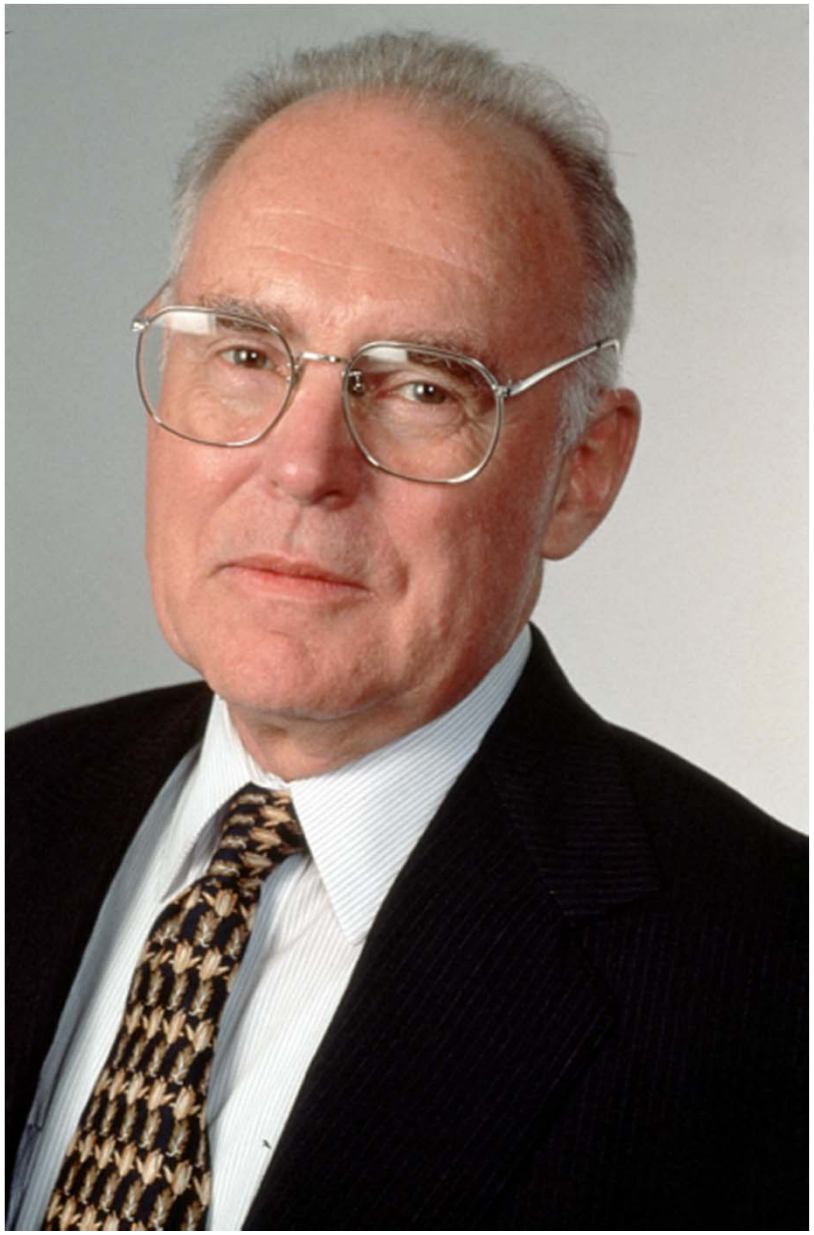
Six-Core Core i7	1,170,000,000	2010	Intel	32 nm	
Dual-Core Itanium 2	1,700,000,000[3]	2006	Intel	90 nm	596 mm²
Six-Core Xeon 7400	1,900,000,000	2008	Intel	45 nm	
Quad-Core Itanium Tukwila	2,000,000,000[4]	2010	Intel	65 nm	
8-Core Xeon Nehalem-EX	2,300,000,000[5]	2010	Intel	45 nm	

GPU transistor count

Processor	Transistor count	Date of introduction	Manufacturer	Process	Area
G80	681,000,000	2006	NVIDIA	90 nm	480 mm²
RV770	956,000,000[6]	2008	AMD	55 nm	260 mm²
RV850	1,040,000,000[7]	2009	AMD	40 nm	170 mm²
GT200	1,400,000,000[8]	2008	NVIDIA	55 nm	576 mm²
RV870	2,154,000,000[9]	2009	AMD	40 nm	334 mm²
GF100	3,000,000,000[10]	2010	NVIDIA	40 nm	529 mm²

Gordon Moore

- The co-founder of Intel
- Famous
  - Because of Moore's law



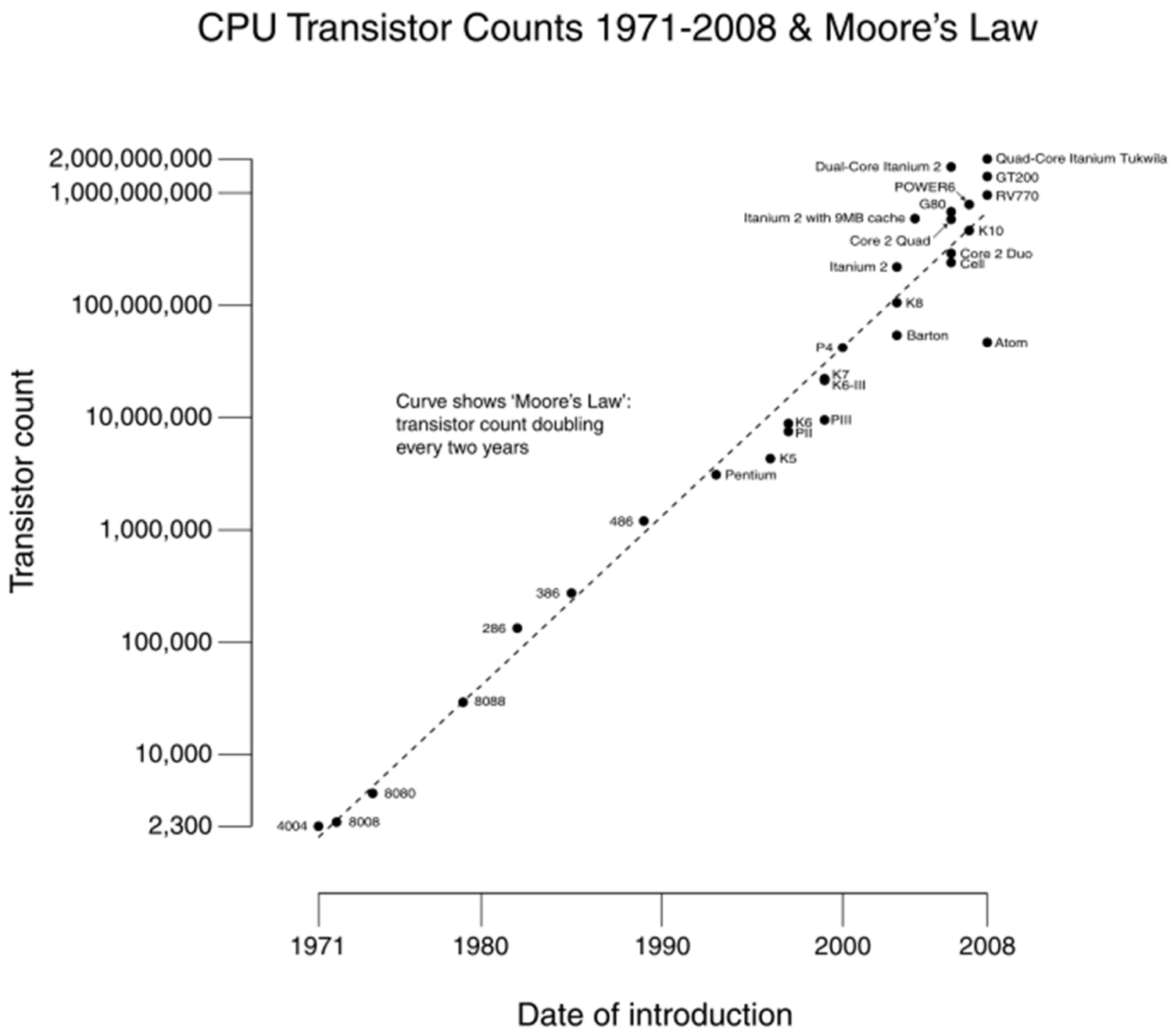
Moore's Law (1)

- 1965
- Number of transistors
  - In commercial CPUs
  - Will be almost DOUBLED
  - Every two years
- In other words
  - Number of transistors per chip:
  - 2 ^ (year – 1959)

Moore's Law (2)

- Number of designers for each CPU
  - Grows as 1/x
  - 4004 had 3 designers
  - Intel dual core has 300 designers
- Fab cost
  - Grows as 1/x
  - 90nm fab costs 2 Billion dollars

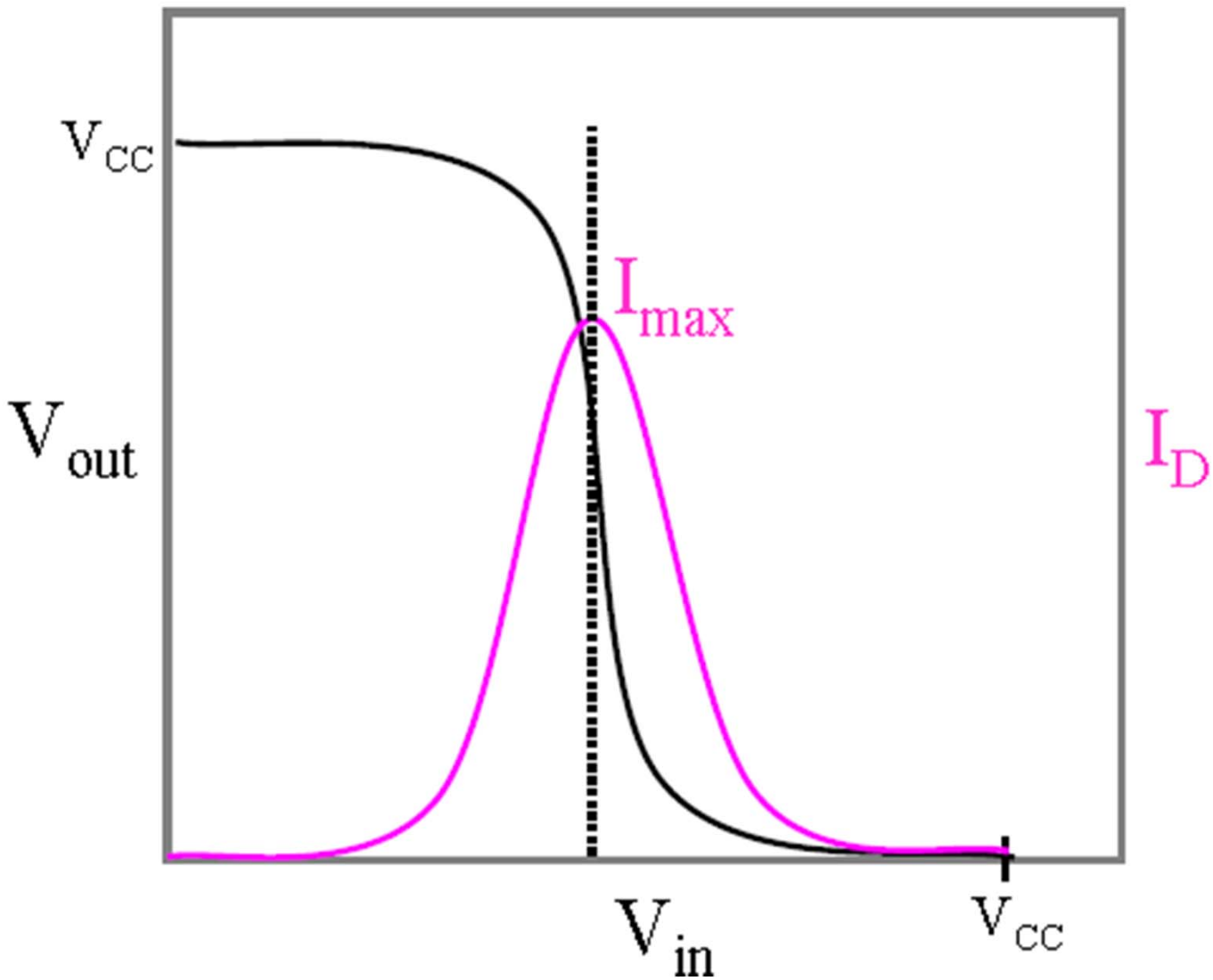
Moore's Law in Practice



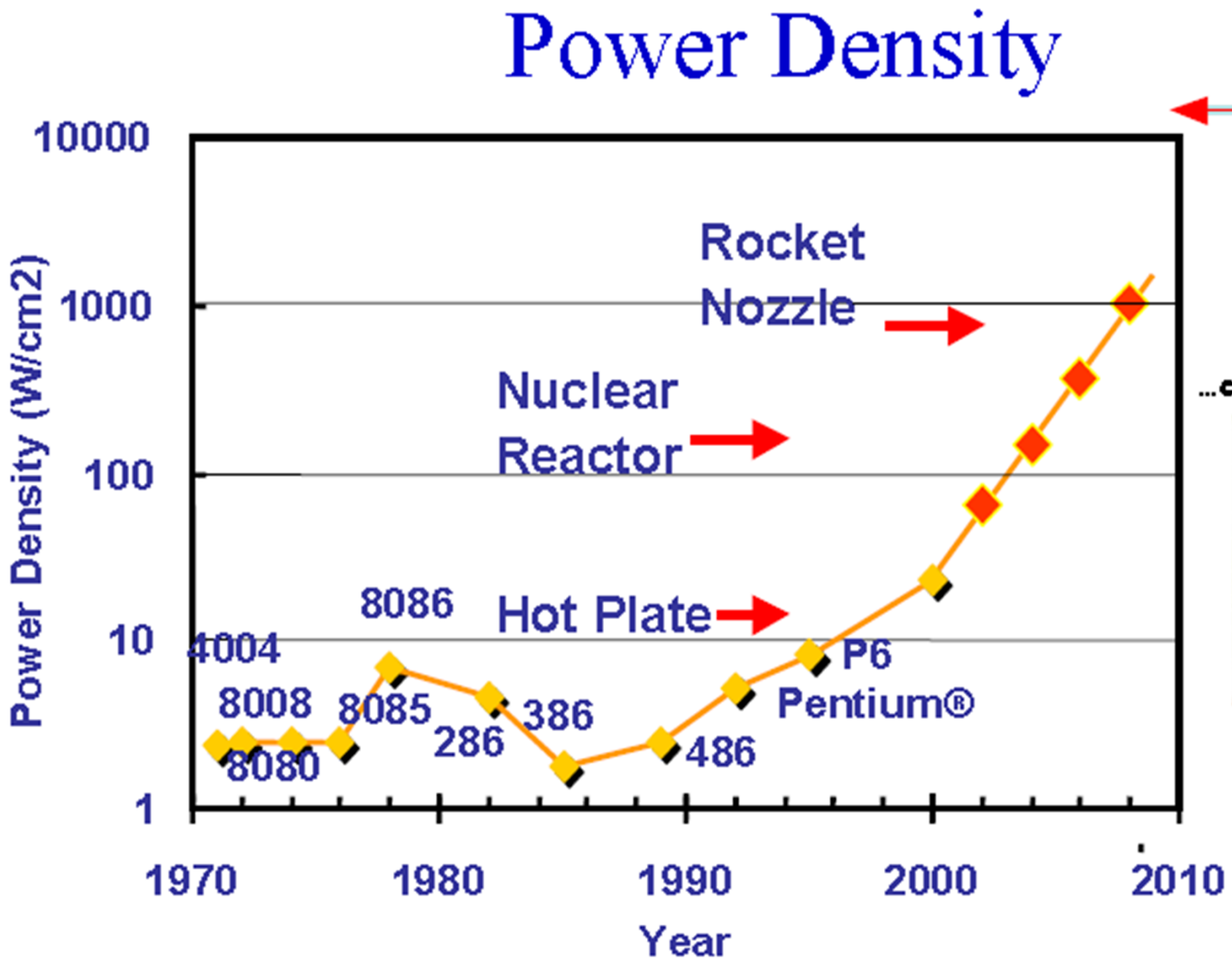
Improving Performance

- How to improve performance
  - Increase transistor count
    - Cache area
    - Parallel units
  - Increase frequency

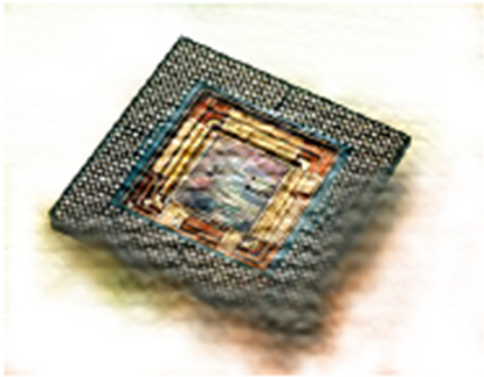
NOT Gate Power Consumption



CPU Power Consumption

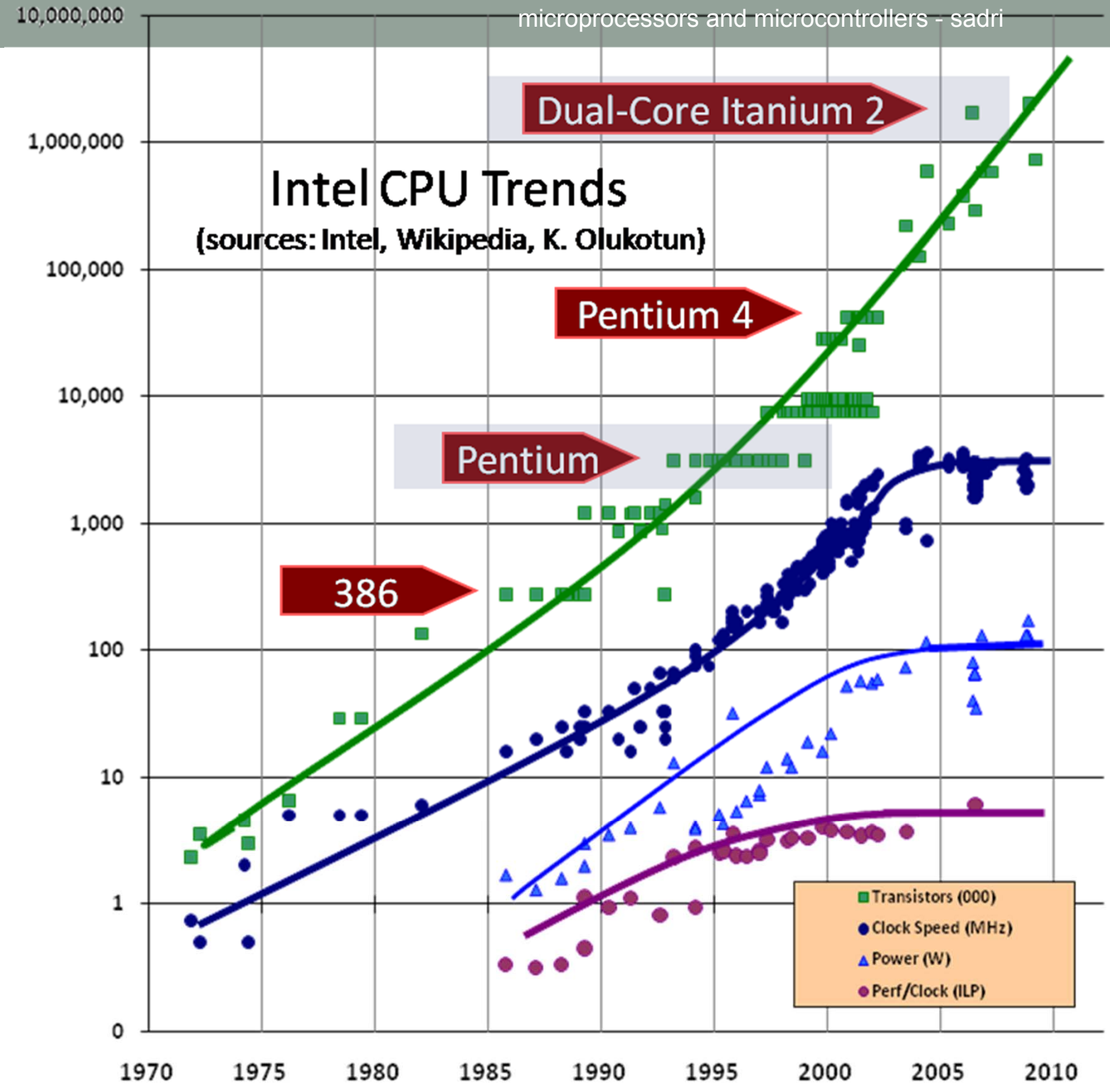


...chips might become hot...



Generated Heat

- Generated Heat is a function of:
  - F : Running frequency
  - V^2 : Supply voltage to the power of 2
- We have to decrease these variables


Intel CPU Trends
(sources: Intel, Wikipedia, K. Olukotun)
Dual-Core Itanium 2
Pentium 4
Pentium
386
10,000,000
1,000,000
100,000
10,000
1,000
100
10
1
0
1970
1975
1980
1985
1990
1995
2000
2005
2010
Transistors (000)
Clock Speed (MHz)
Power (W)
Perf/Clock (ILP)

MULTI CORE COMPUTING

Chapter 3