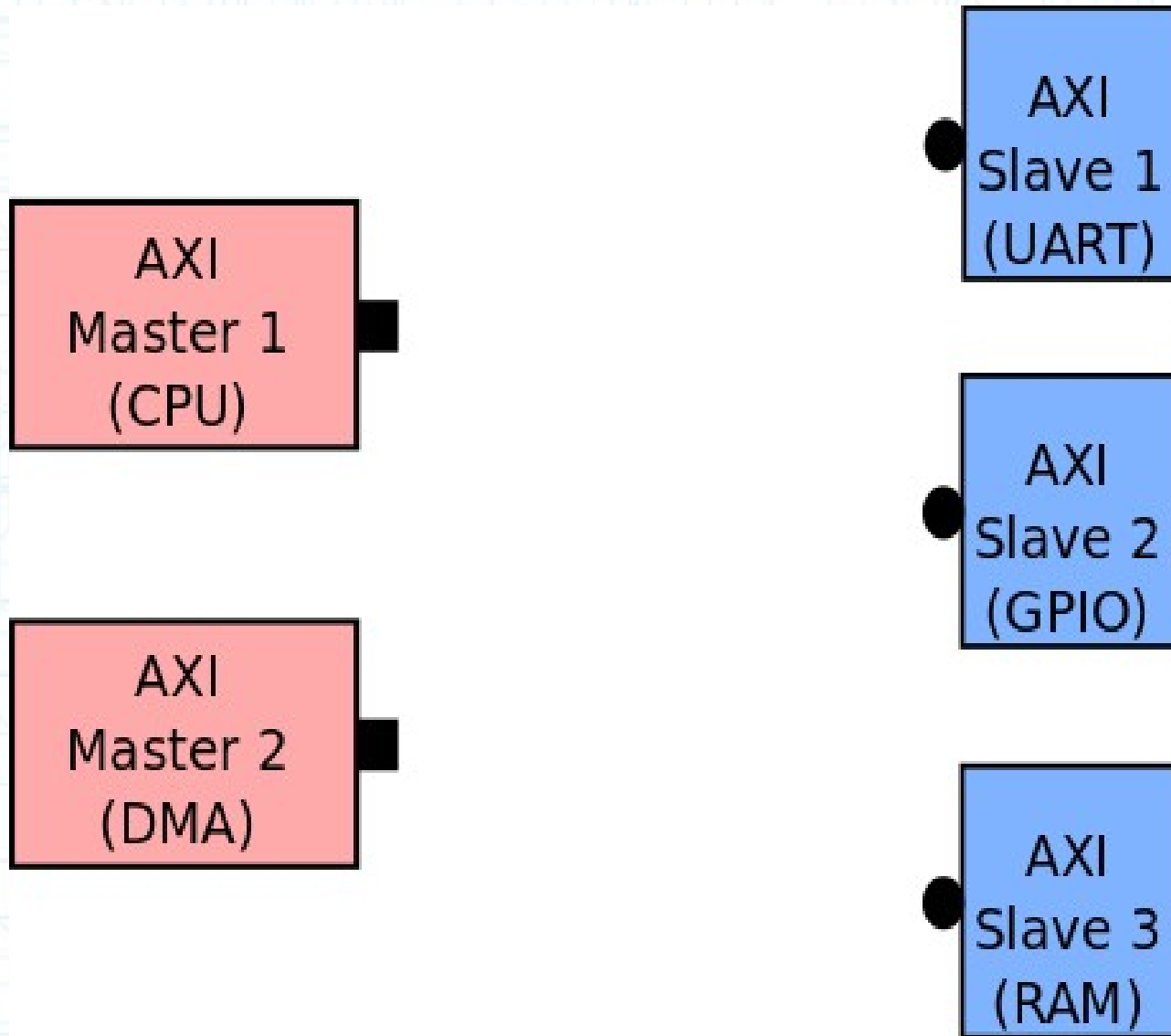


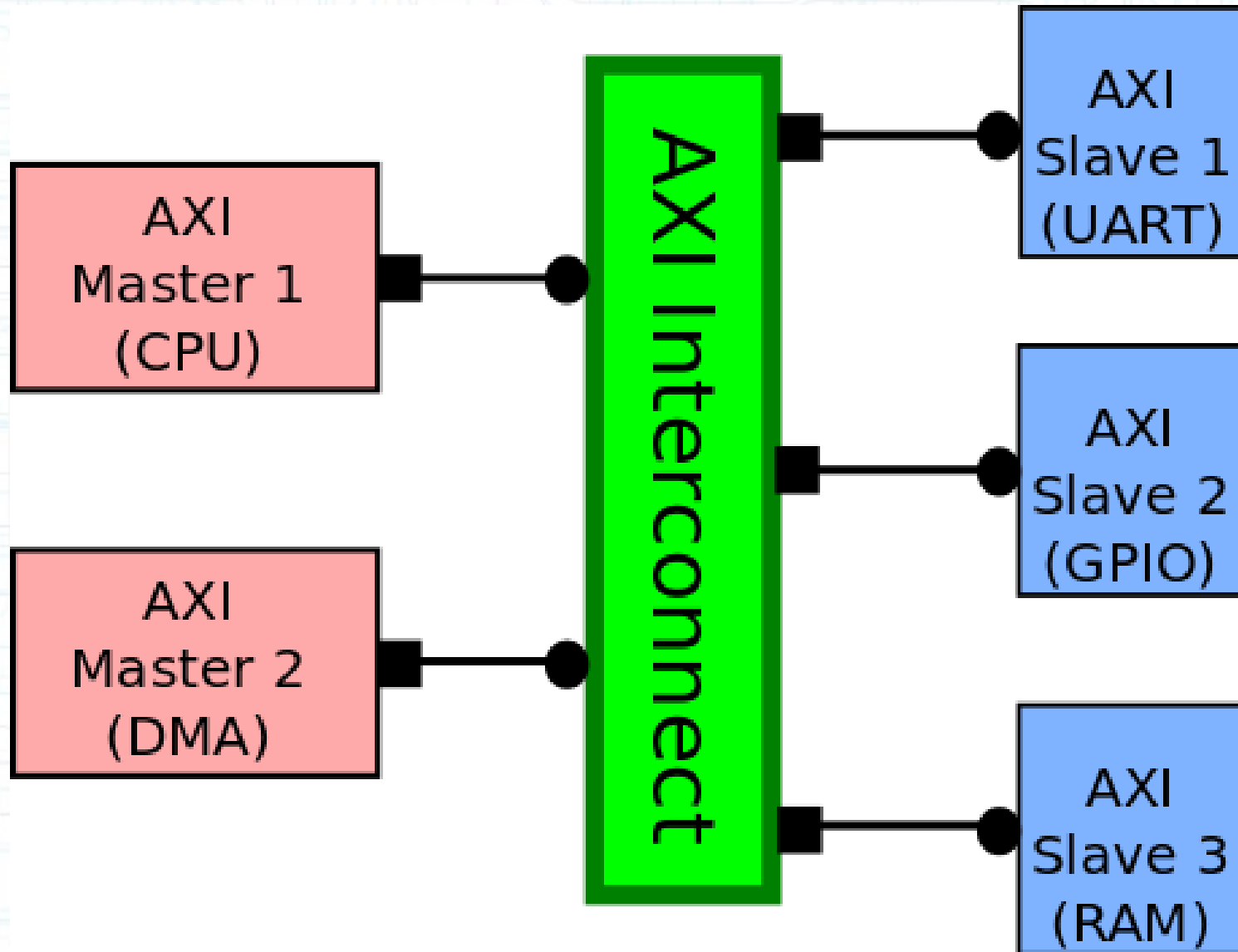
# What is an AXI Interconnect?

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March – 20 - 2014

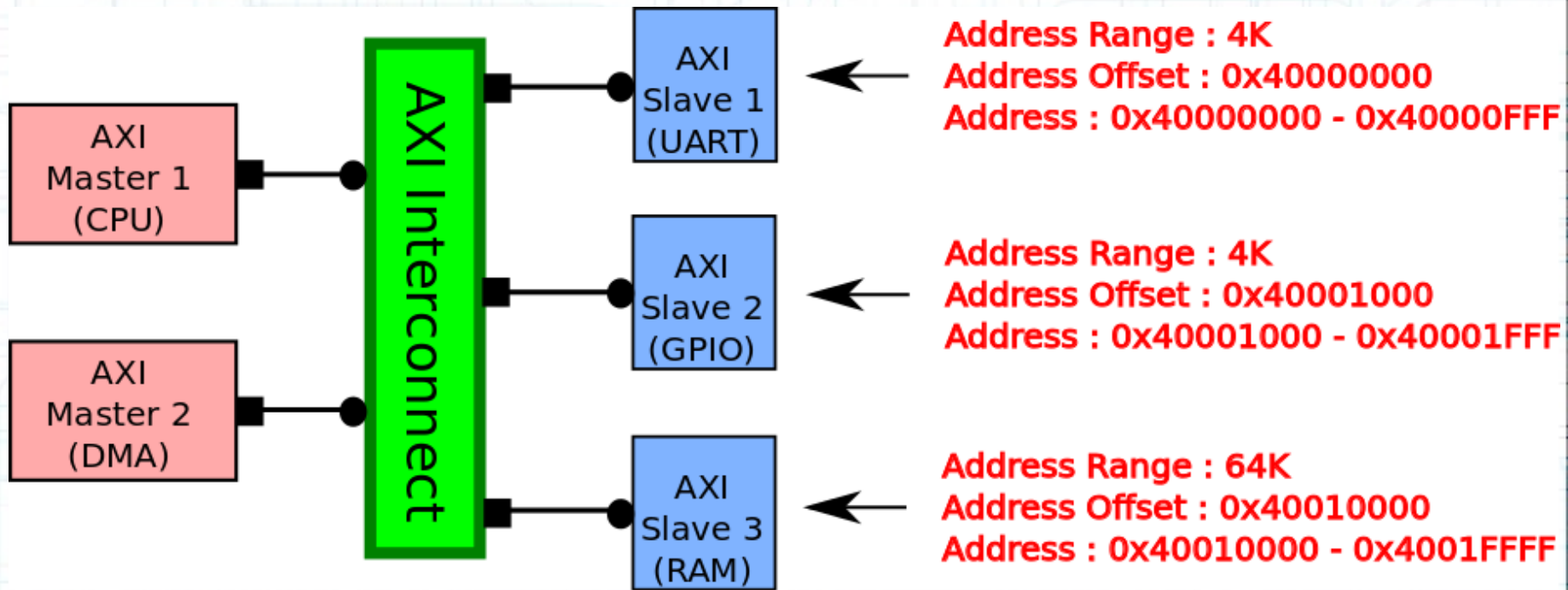
# Connecting Masters & Slaves



# AXI Interconnect



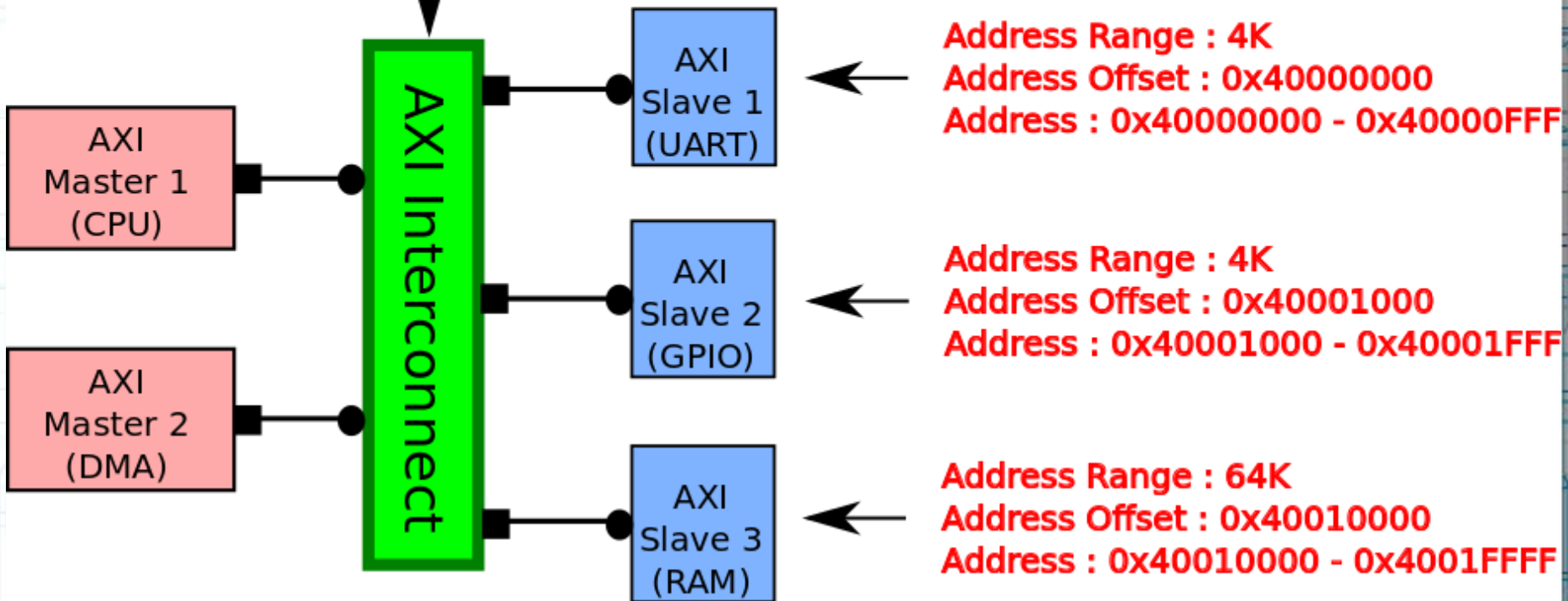
# Addressing...



# AXI Interconnect Address Decoding

Address Decoding Table

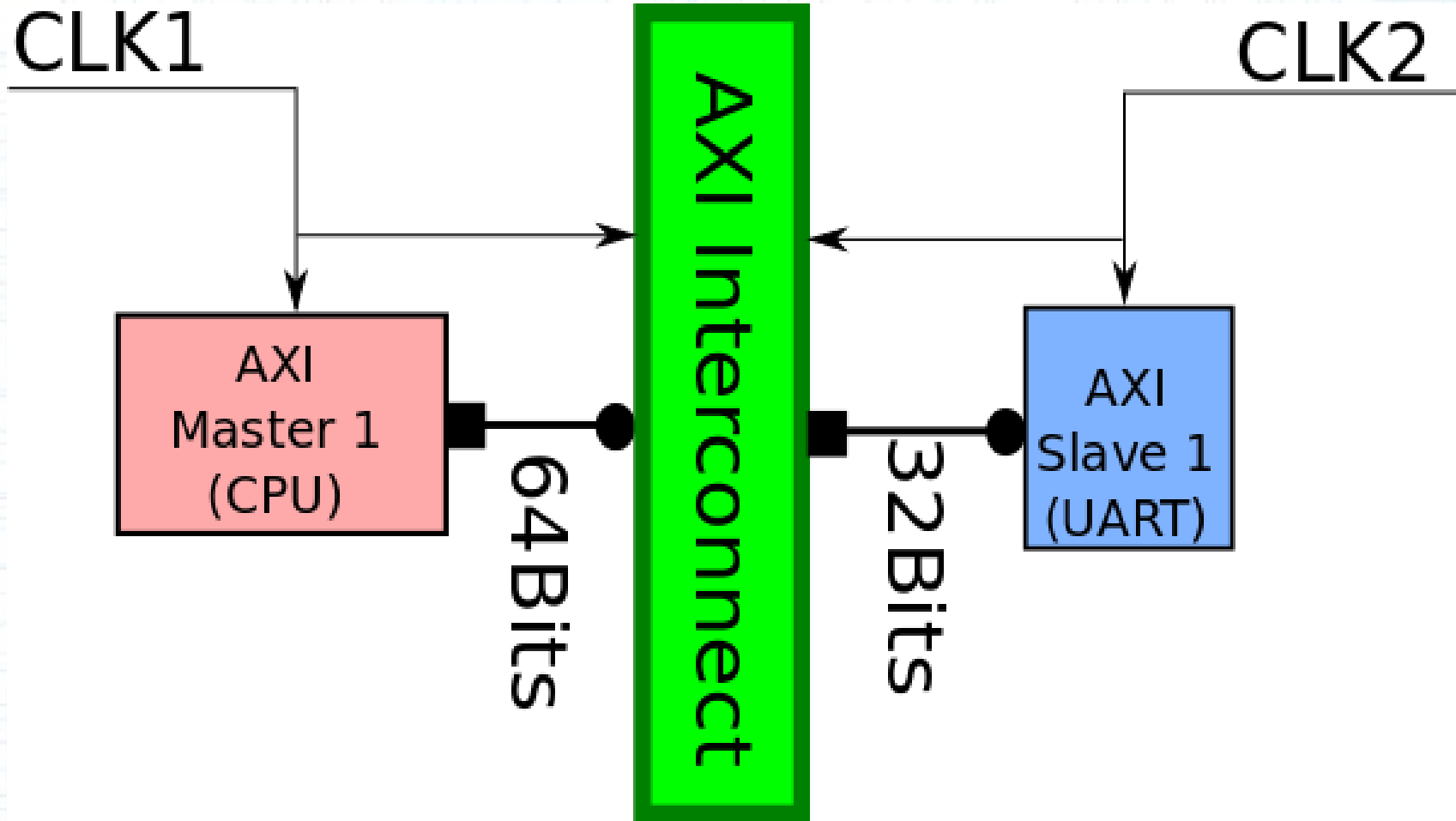
UART : 0x40000000 - 0x40000FFF
GPIO : 0x40001000 - 0x40001FFF
RAM : 0x40010000 - 0x4001FFFF



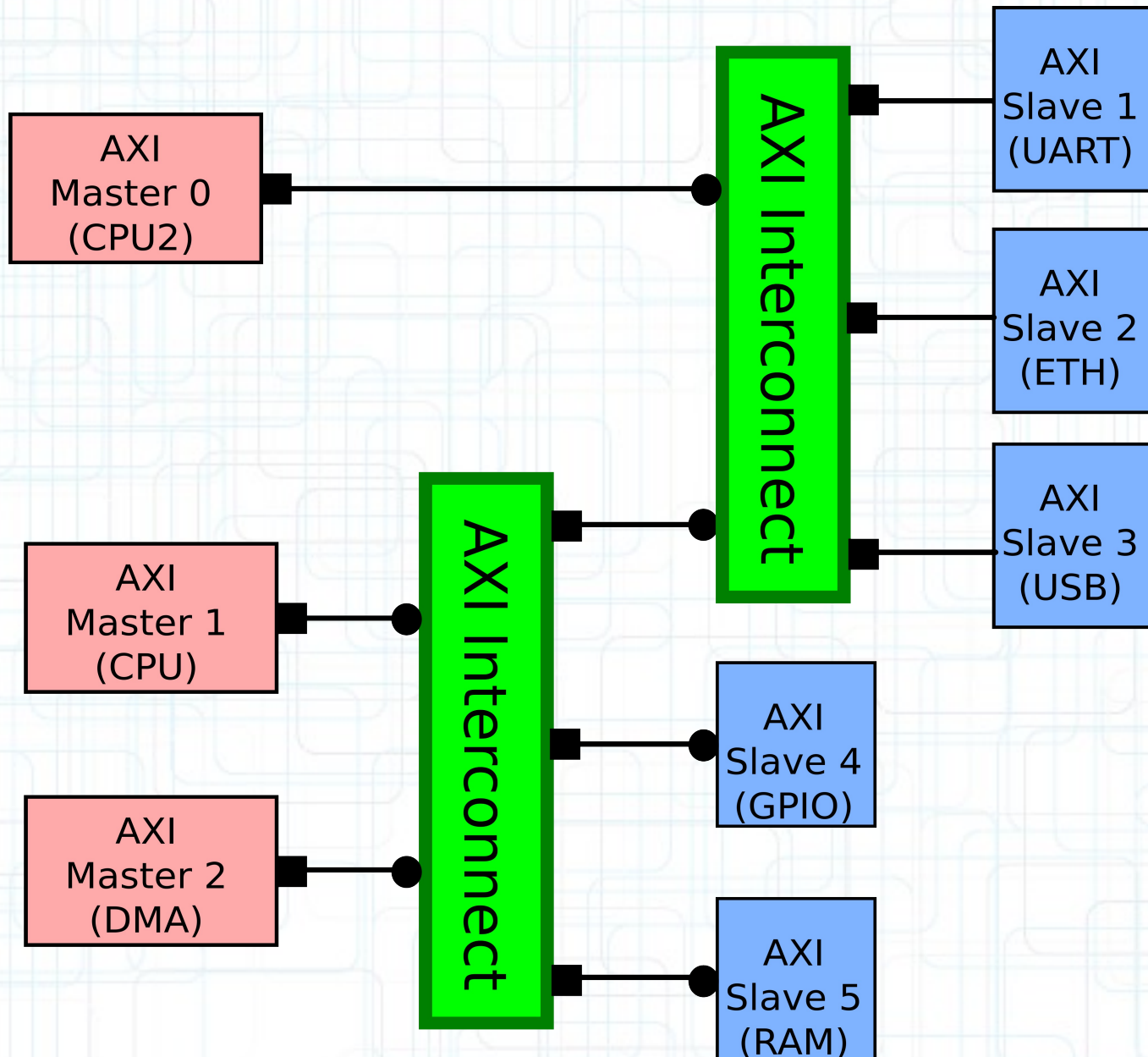
# AXI Interconnect

- Different number of
  - Slave and Master Ports
- Width Conversion
- AXI3 to AXI4
- Register slices, Input/output FIFOs
- Clock Domain Transformation

# AXI Interconnect



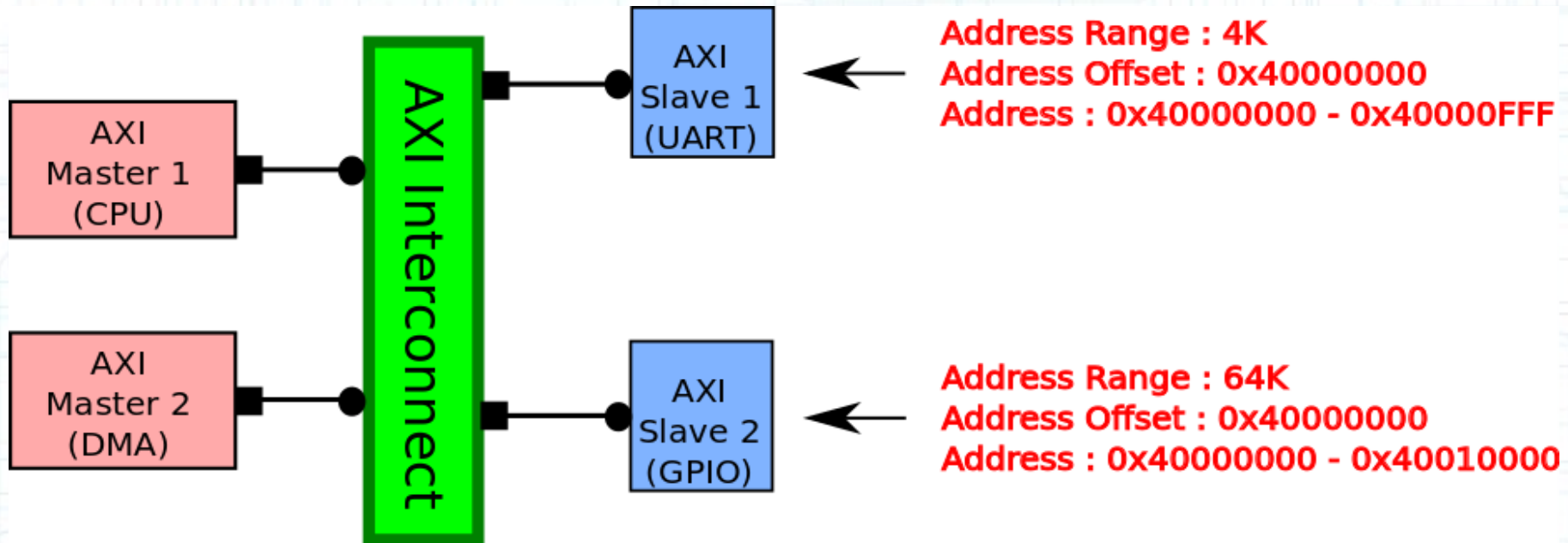
# Hierarchical AXI Interconnects





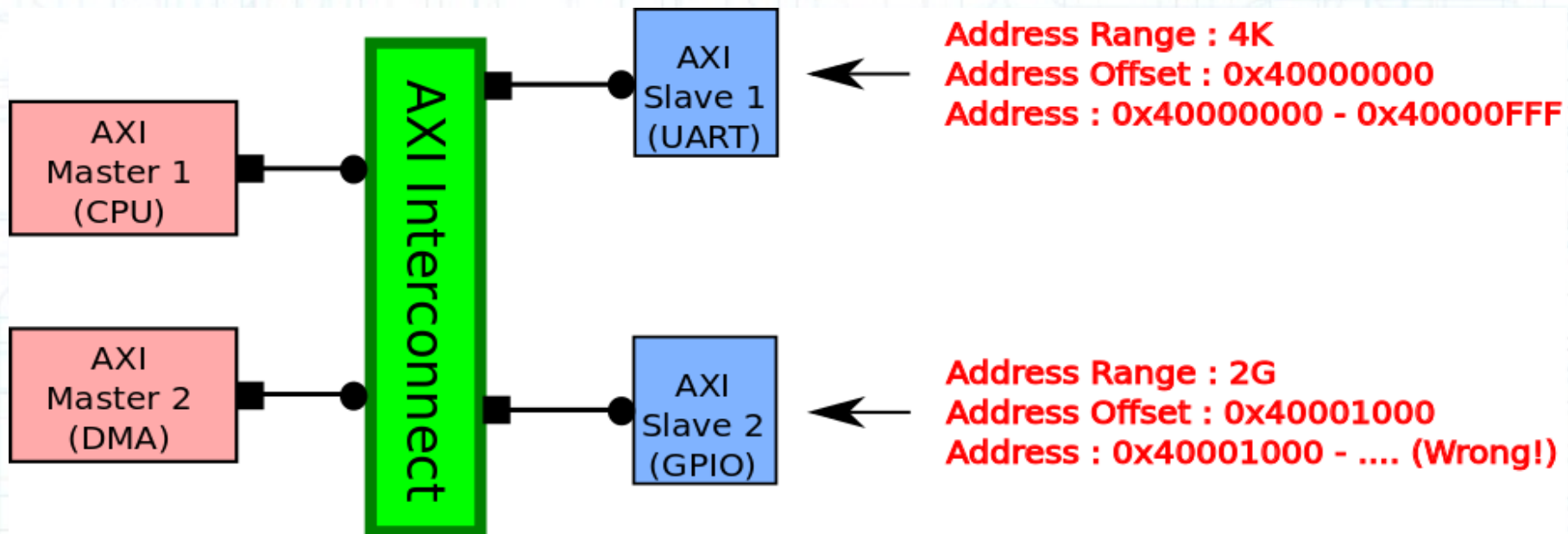
# Simple Address Definition Rules

- No overlaps



# Simple Address Definition Rules

- Meet required alignment in Address



Correct : Offset should be in 2G  
Boundary ! e.g. 0xC0000000

# Thanks ...

**This is a personal hobby! But I would like to thank**

- Prof. Luca Benini, of University of Bologna & ETHZ**
- Prof. Norbert Wehn of TU Kaiserslautern**

## Latest Material ...

**My personal web sites :**

**[www.green-electrons.com](http://www.green-electrons.com)**

**[www.googoolia.com](http://www.googoolia.com)**