

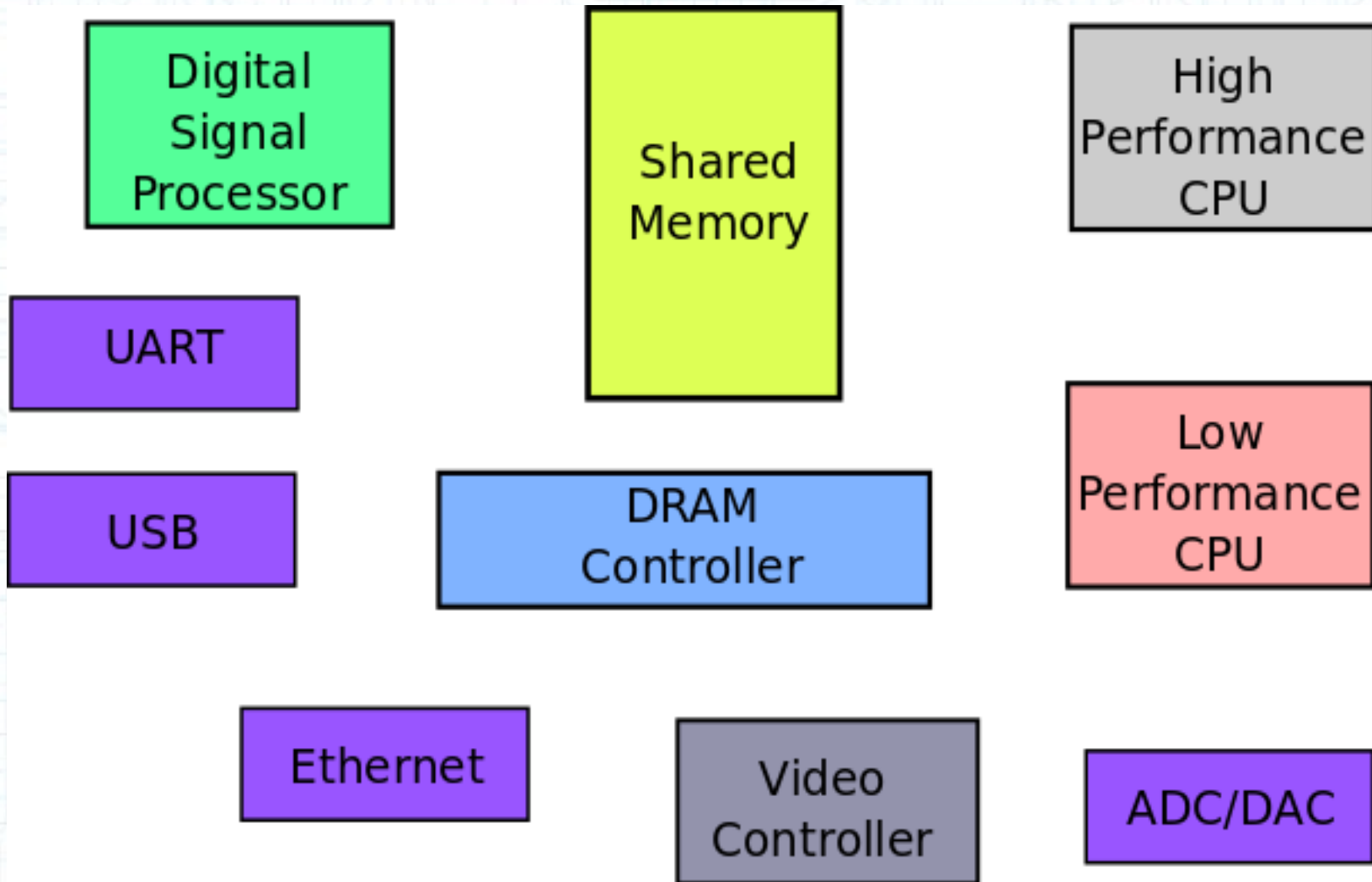
What is AXI?

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Introduction

- Getting familiar with ZYNQ design flow
 - Need knowledge of AXI
- Good knowledge on AXI
 - Fast and efficient development with Vivado!

Today's System-On-Chips!

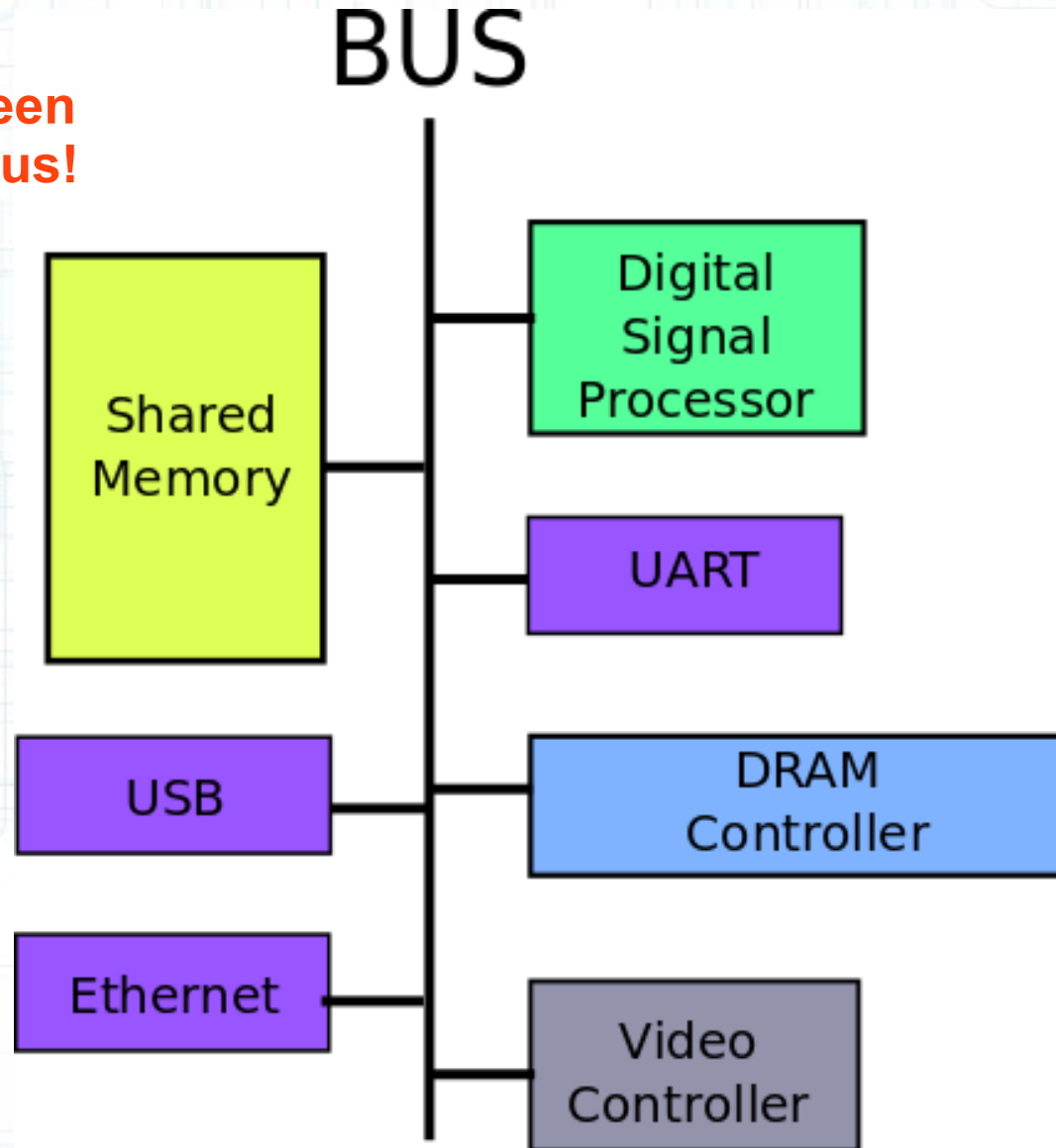


Connectivity!

- A standard
 - All units talk based on that standard
 - All units can talk easily to each other
- Maintenance
 - Design is easily maintained/updated, debugged
- Re-use
 - Units can be easily re-used in other designs

System-On-Chip Buses !

A Standard Way of
Communication between
The Module and the Bus!



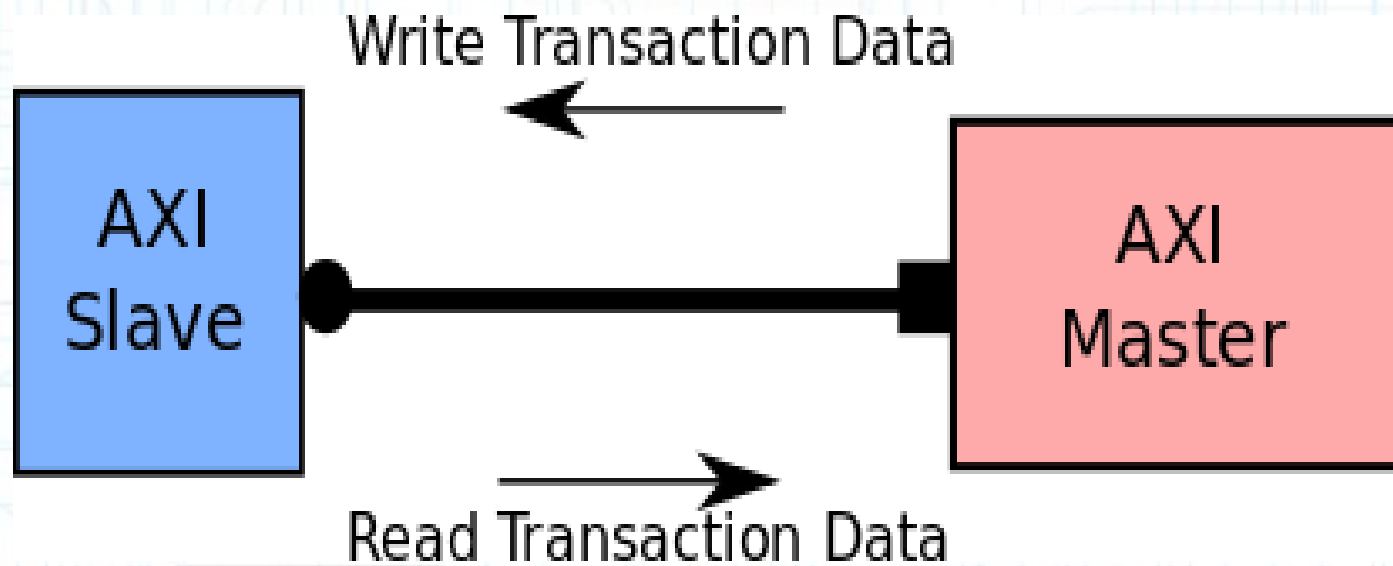
Famous SoC Buses!

- Core-Connect
 - PLB/OPB/.....
- WishBone
 - Used by OpenCore Ips
- AXI
 - Developed by ARM

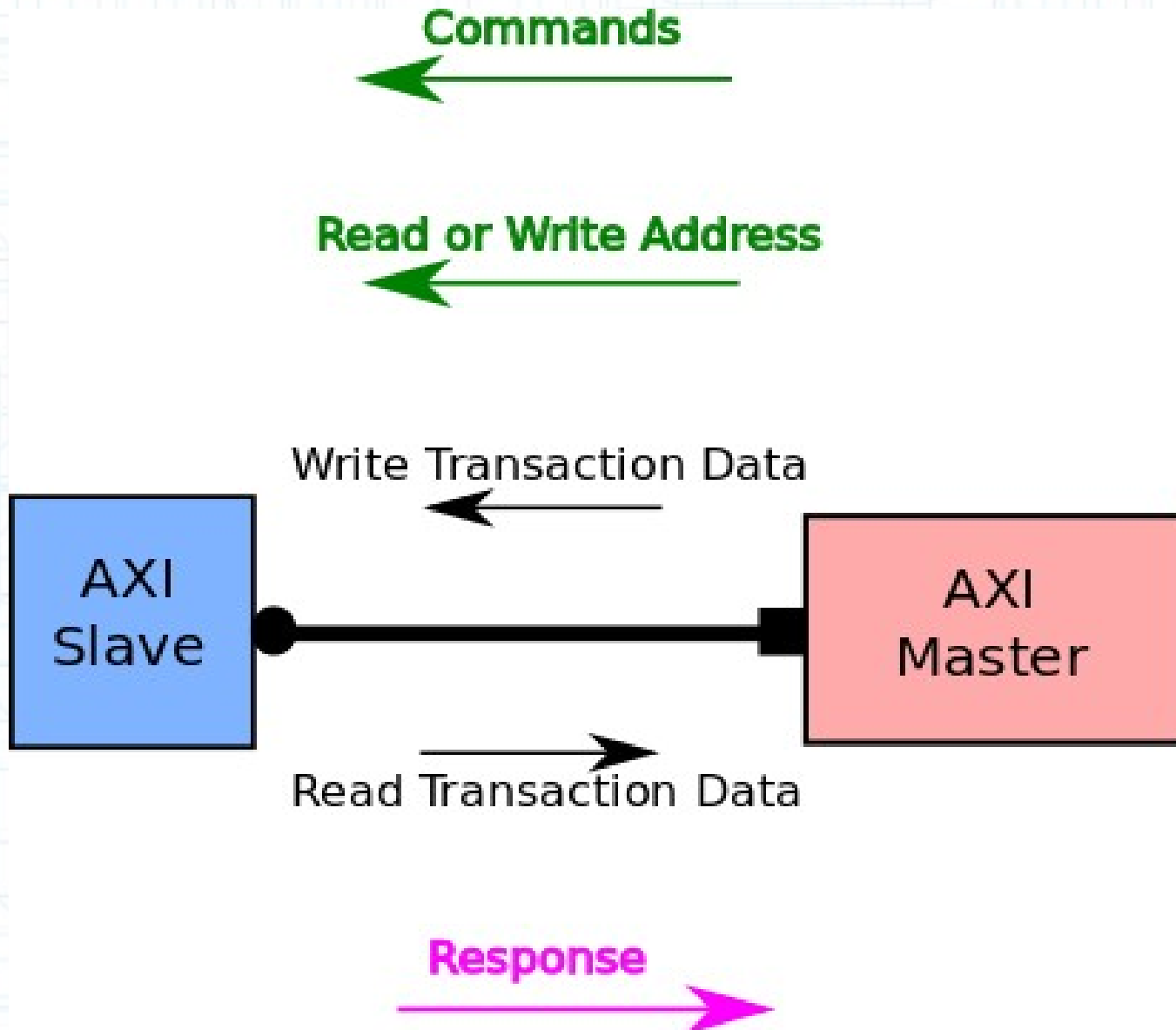
AXI Master / AXI Slave

- Transaction :
 - Transfer of data from one point in the hardware to another point
- Master : Initiates the transaction
- Slave : Responds to the initiated transaction

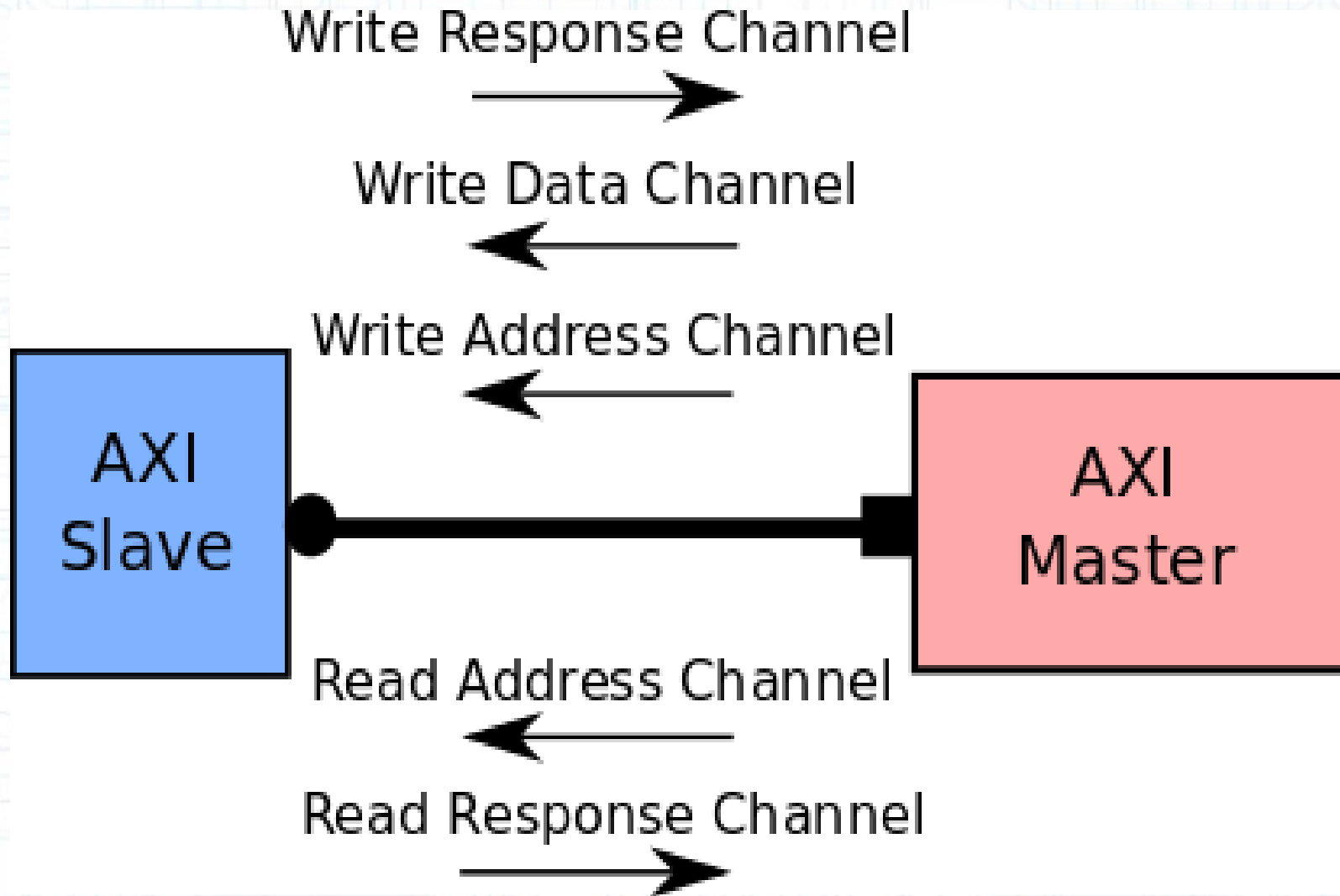
AXI Master / AXI Slave



AXI Master / AXI Slave



The 5 Channels of AXI Interface



AXI Interconnect

- What if
 - One AXI Master wanted to talk to two AXI slaves?
 - Two AXI Masters to One AXI slave?
 - ...

Thanks ...

This is a personal hobby! But I would like to thank

- Prof. Luca Benini, of University of Bologna & ETHZ**
- Prof. Norbert Wehn of TU Kaiserslautern**

Latest Material ...

My personal web sites :

www.green-electrons.com

www.googoolia.com