Designing with AXI using Xilinx Vivado Environment (Part II)

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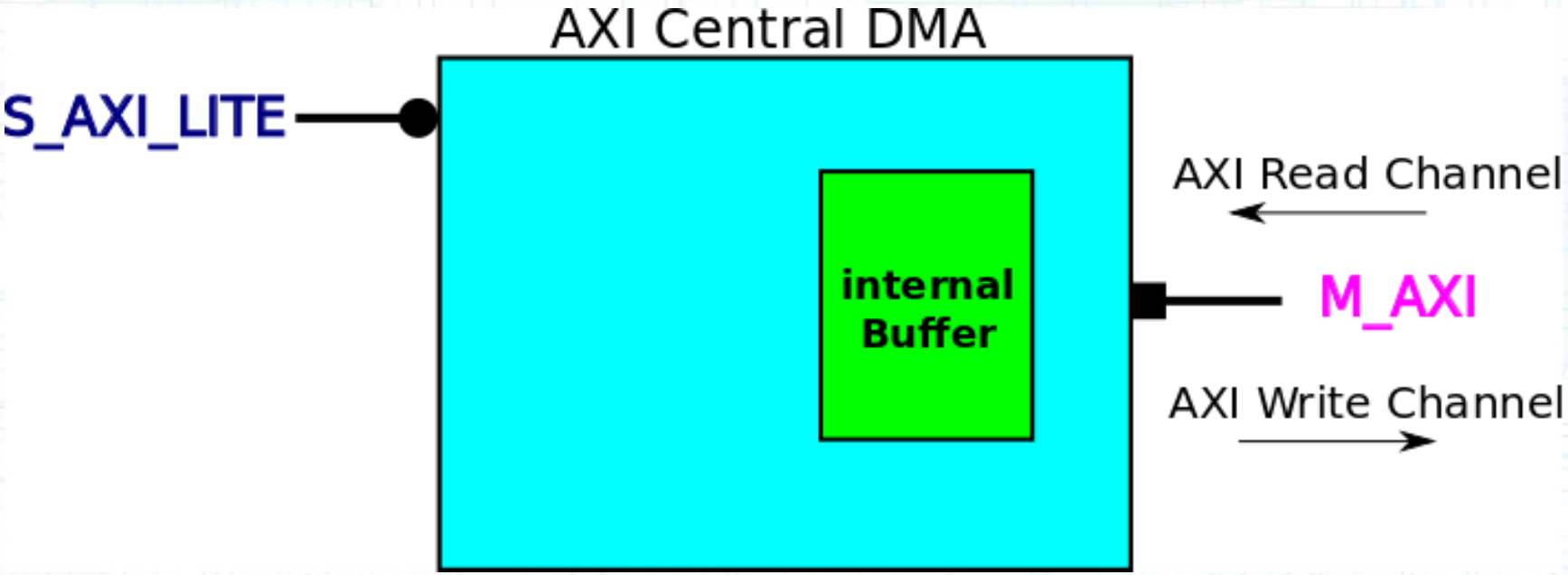
Previous Lesson

- Introduction to Vivado
- Using MicroBlaze CPU Core in Vivado
- Designing an example AXI architecture

This Lesson

- Further practical examples using Vivado
  - Design rules for addresses of different components
- Rest of the design flow : synthesis...
- Generating Packaged IP out of Vivado design
  - Packaged IP from HDL source code
    - Vivado Project
  - Packaged IP from Vivado Block Diagram

AXI Central DMA



Thanks ...

This is a personal hobby! But I would like to thank

- Prof. Luca Benini, of University of Bologna & ETHZ

- Prof. Norbert Wehn of TU Kaiserslautern

Latest Material ...

My personal web sites :

www.green-electrons.com

www.googoolia.com